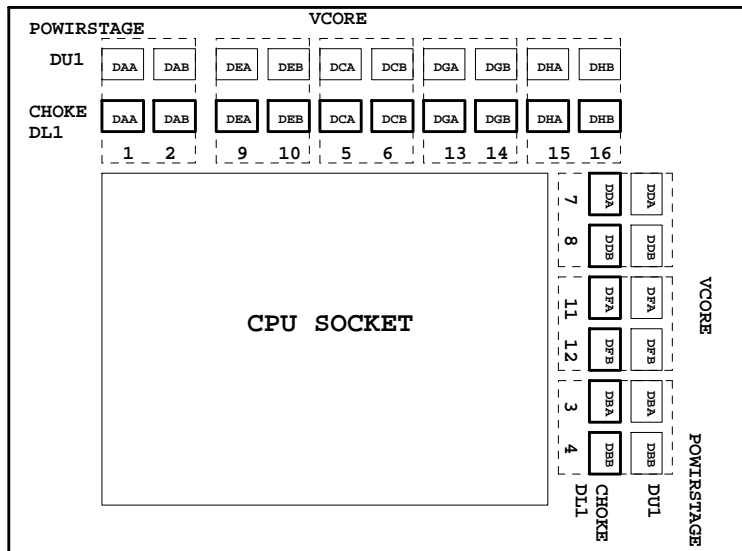


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	DP / DVI / HDMI
15	PCI EXPRESS*16/*8 SWITCH
16	PCI EXPRESS*16 SLOT
17	PCI EXPRESS*8 SLOT
18	PCI EXPRESS*4 SLOT
19	PCI EXPRESS*1 SLOTS X3
20	ITE 8892
21	PCI SLOT 1
22	SATA3 SWITCH
23	USB3_eSATA, KB_USB3
24	Marvell 9172
25	ALC898
26	REAR AUDIO JACK
27	Headphone Audio Amplifier
28	IR3563B PWM Controller
29	IR3553 Power Stage PH_01-04
30	IR3553 Power Stage PH_05-08
31	IR3553 Power Stage PH_09-12
32	IR3553 Power Stage PH_13-16
33	IR3570_DDR PWM Controller
34	IR3598-DDR Driver

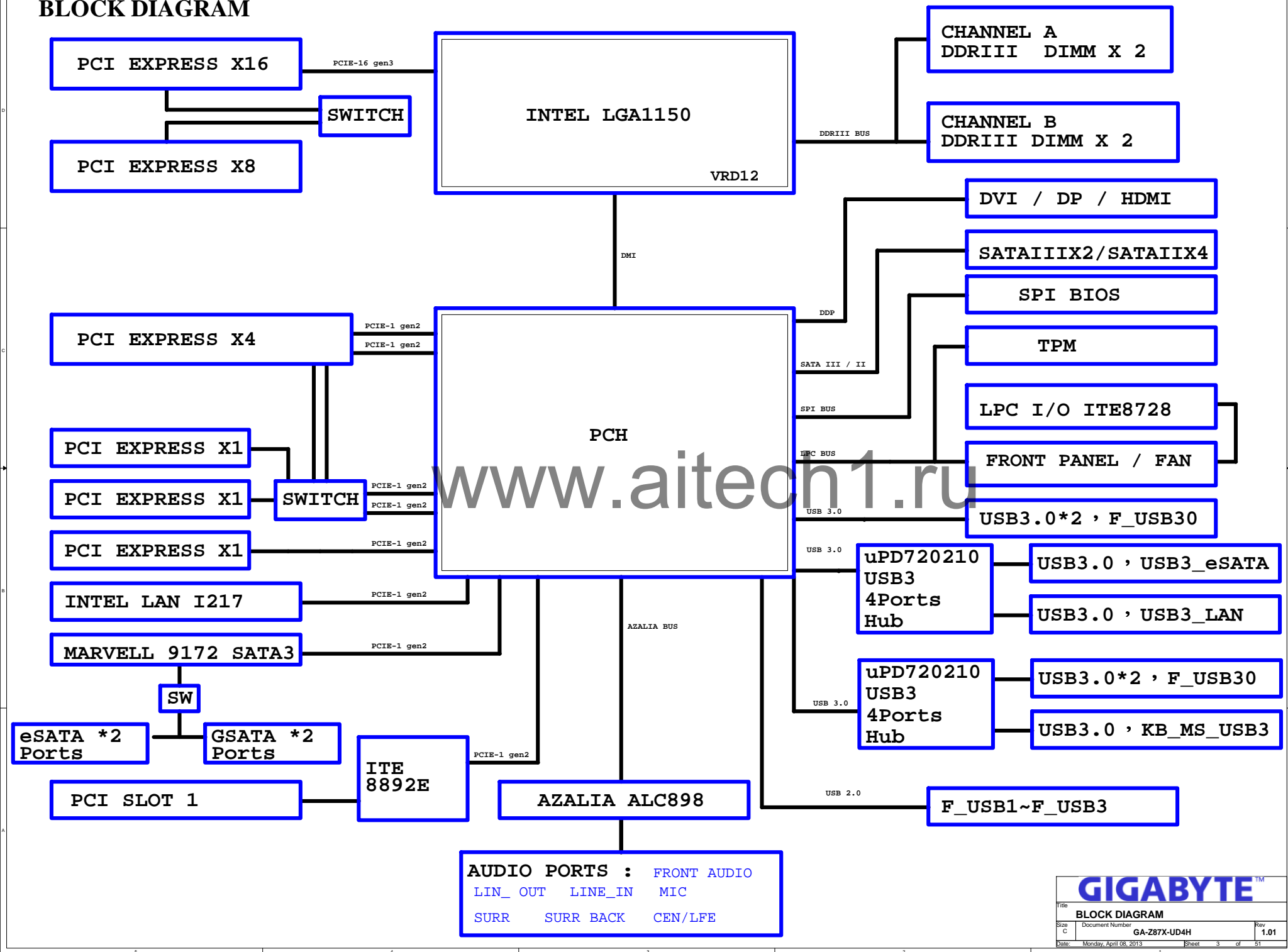
35	DISCRETE POWER I
36	DISCRETE POWER II
37	INTEL LAN I217
38	uPD720210 USB3 4Ports Hub-1A
39	uPD720210 USB3 4Ports Hub-1B
40	F_USB 3.0 from PCH
41	F_USB 2.0
42	Dual BIOS
43	ITE8728 LPC I/O
44	FAN CTRL, H/W Monitor
45	F_PANEL , COM, PROCHOT#
46	Port80, O.V., Voltage Measure
47	ATX POWER, CLOCK GEN
48	TABLE LIST
49	uPD720210 USB3 4Ports Hub-2A
50	uPD720210 USB3 4Ports Hub-2b
51	VCC1_05_ME, VCC3_ME

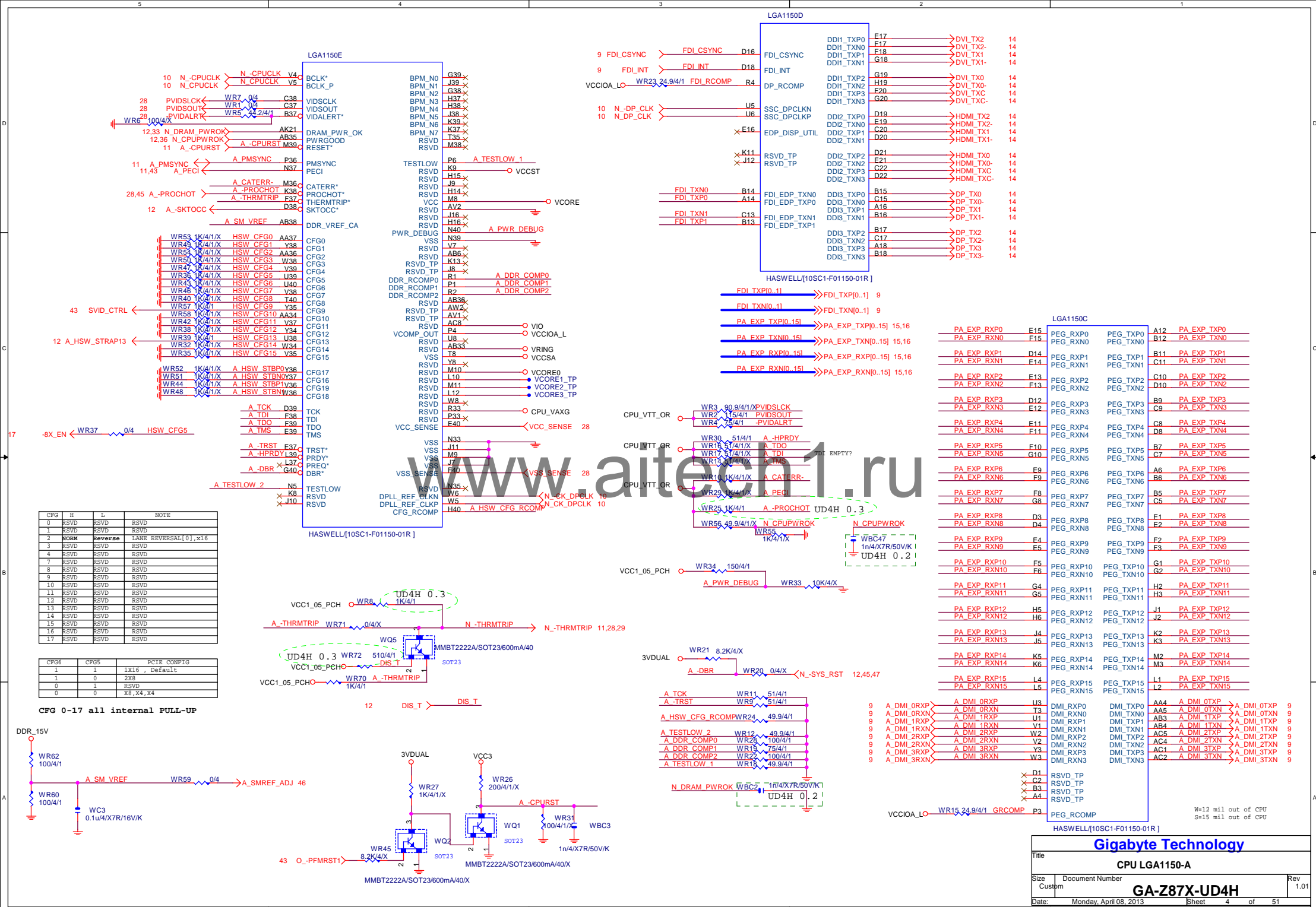


Gigabyte Technology

Title			Cover Sheet
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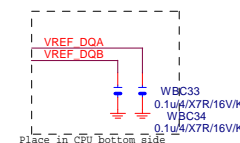
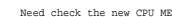
BLOCK DIAGRAM

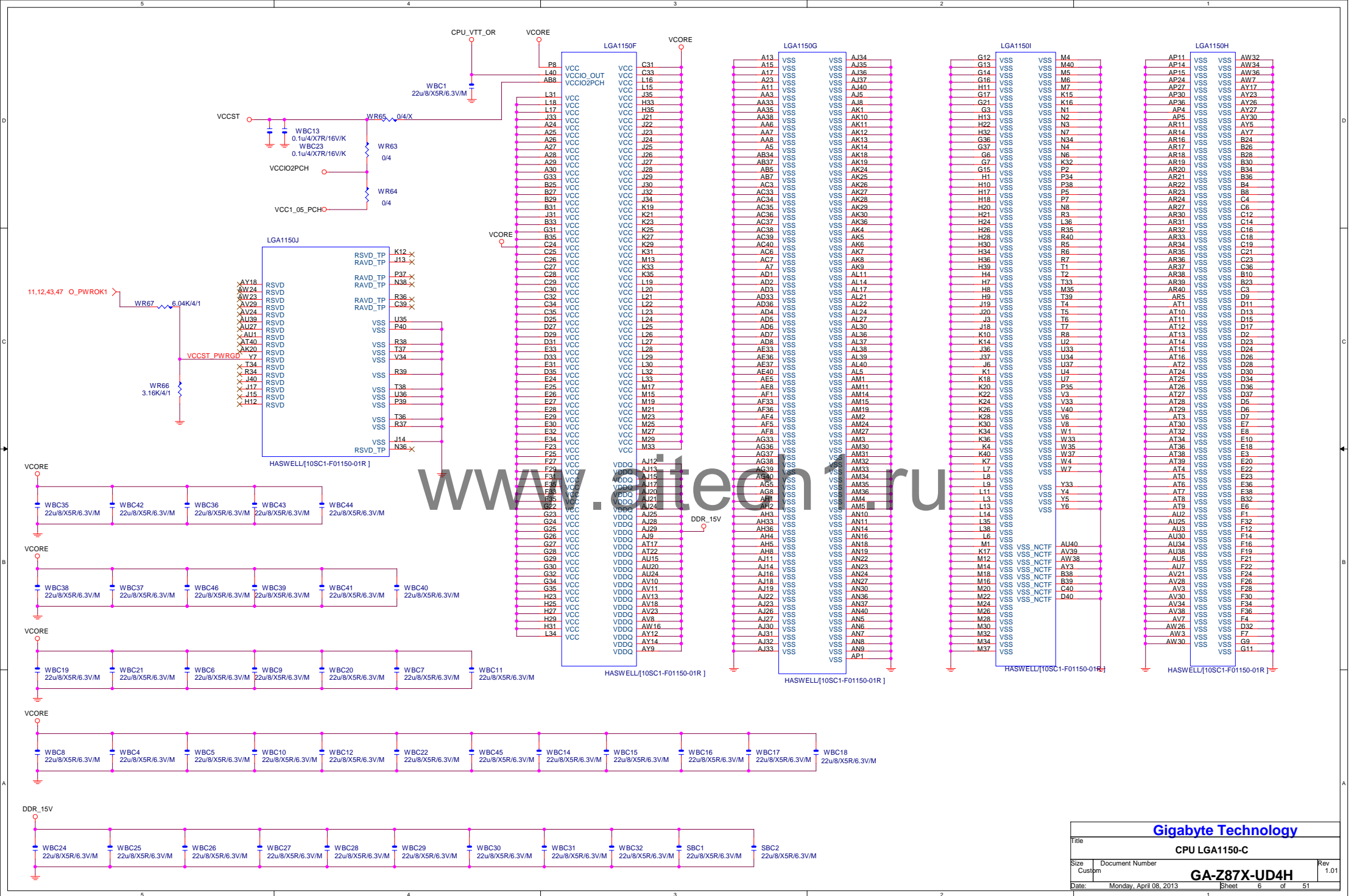


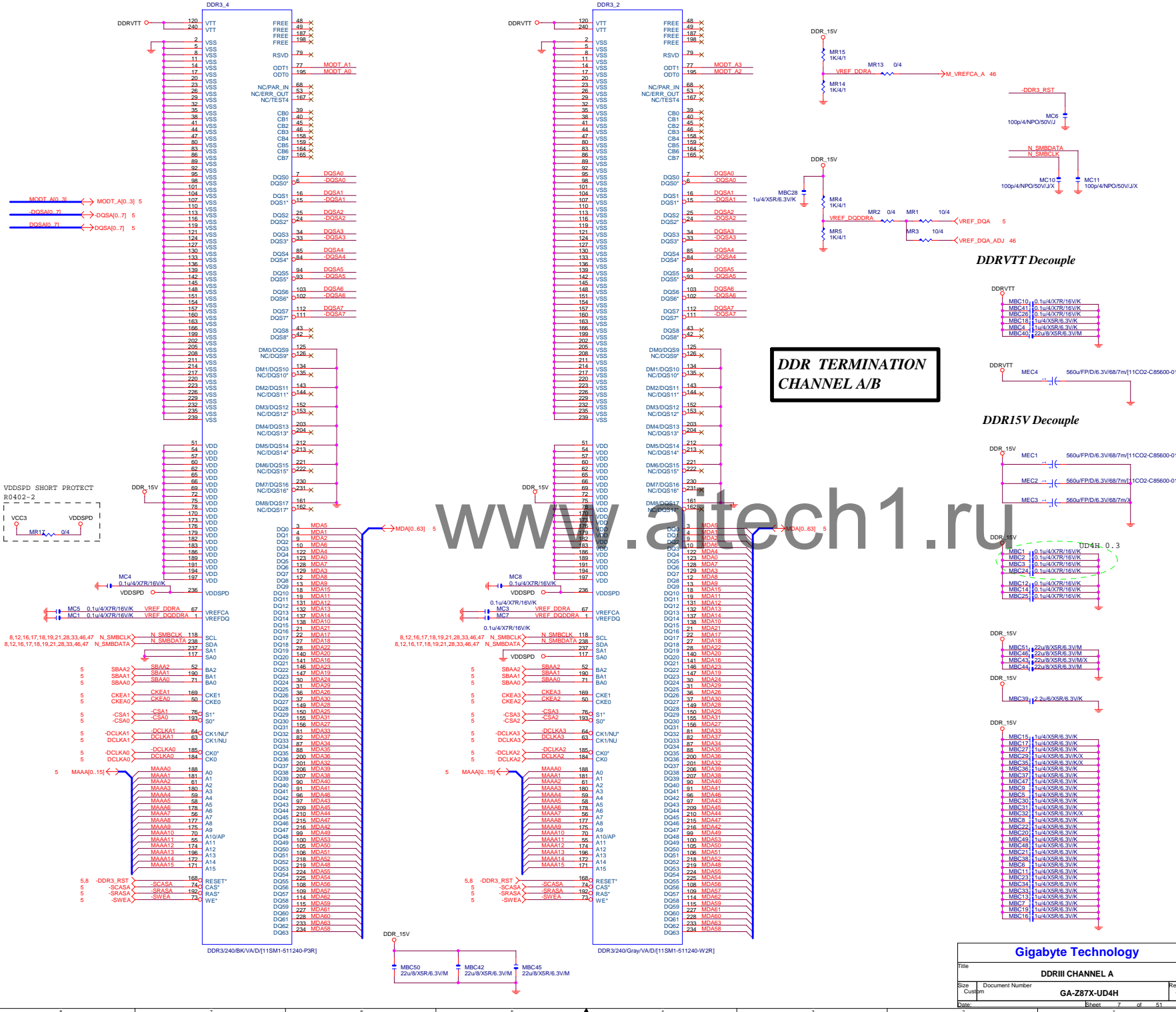


HASWELL/[10SC1-F01150-01R]

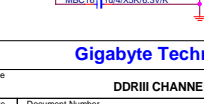
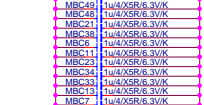
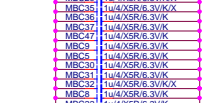
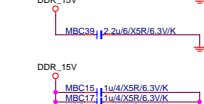
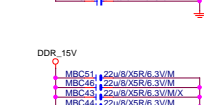
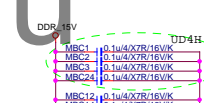
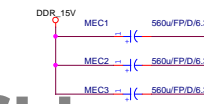
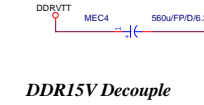
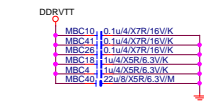
HASWELL/[10SC1-F01150-01R



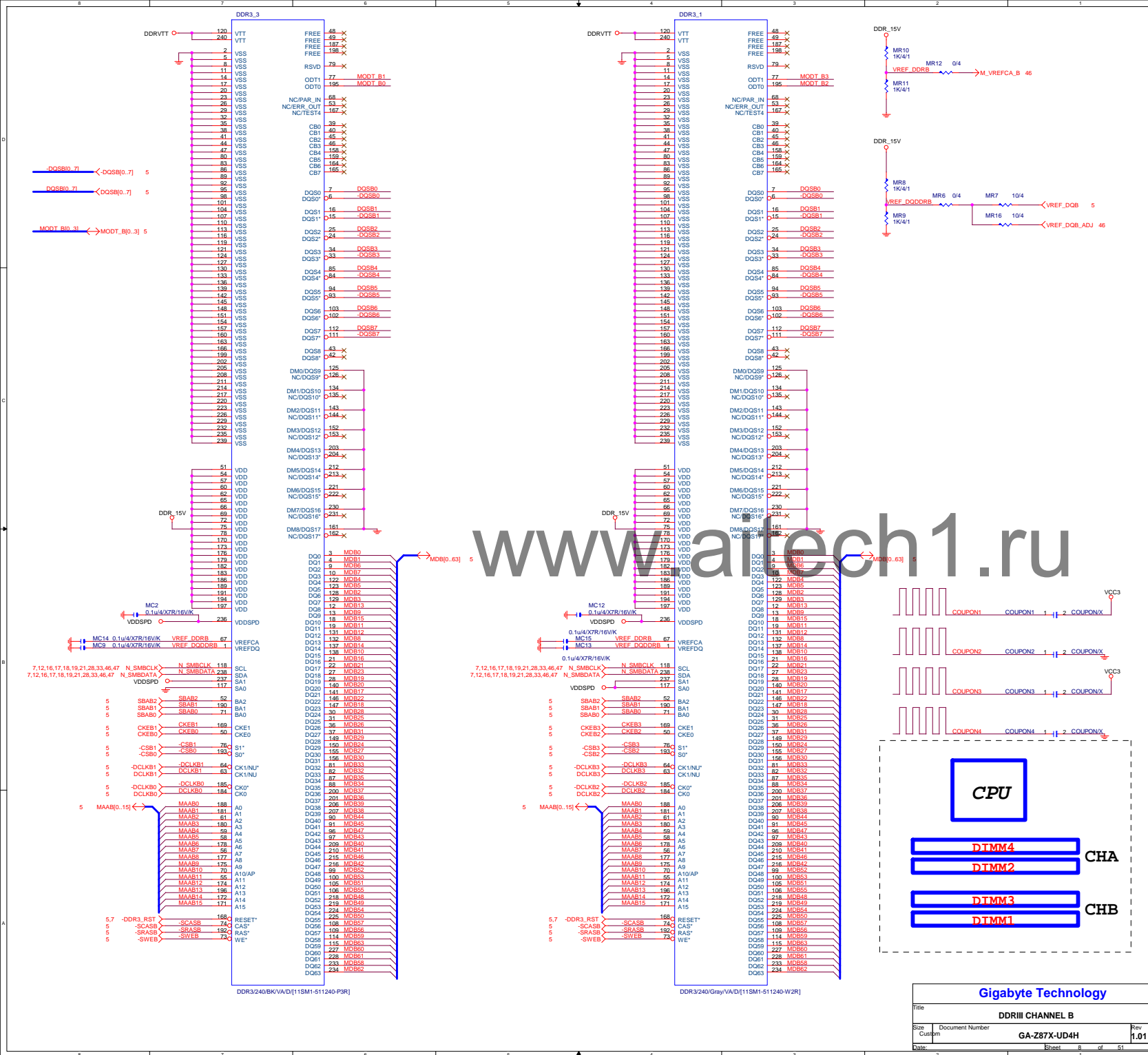


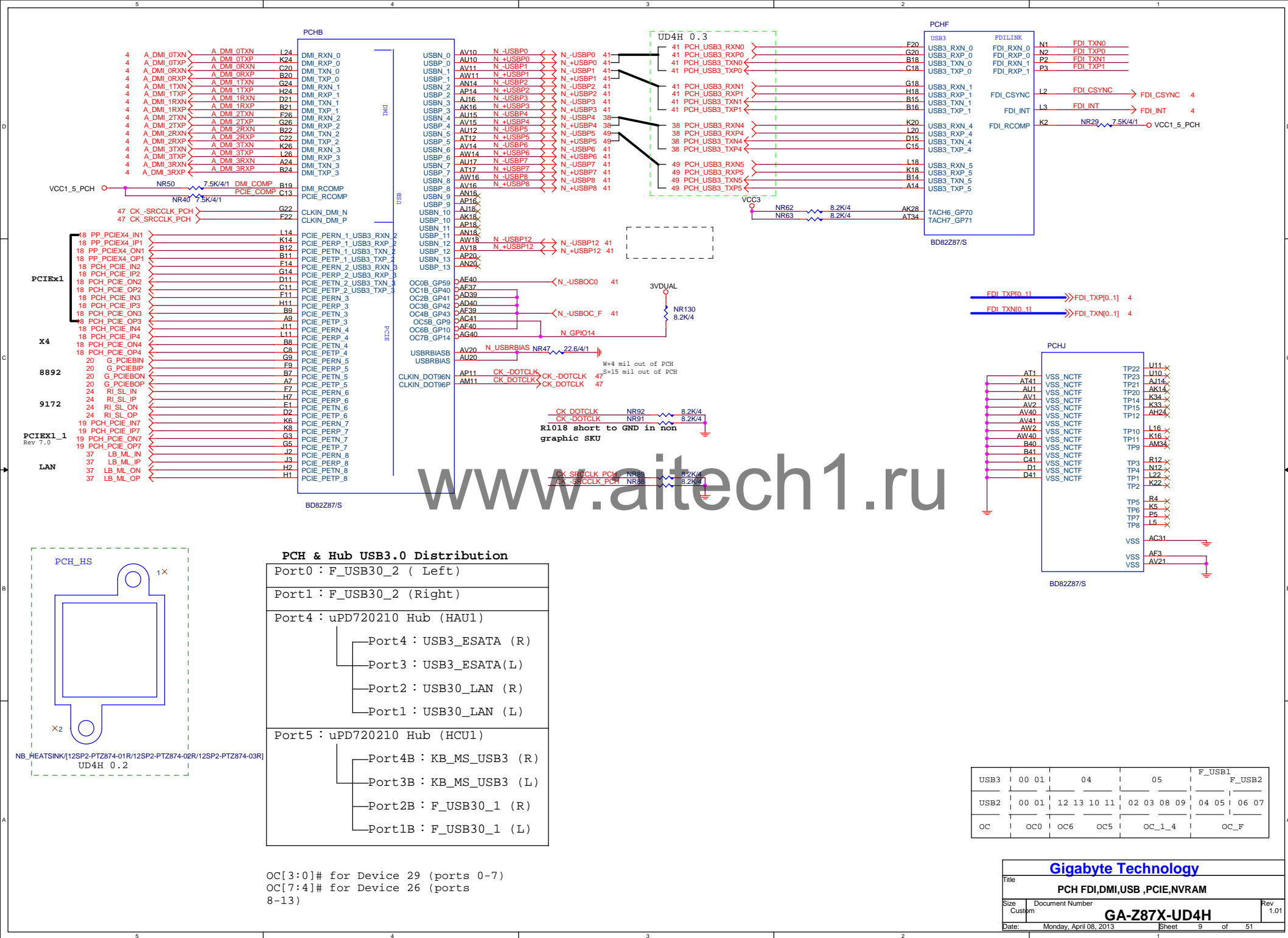


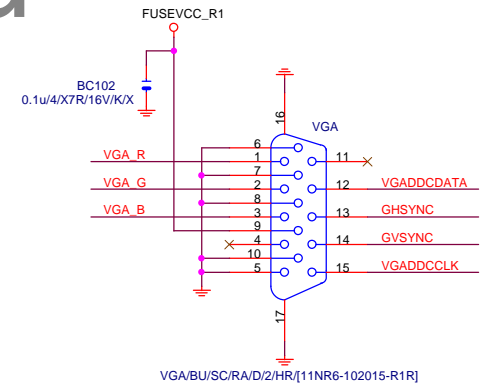
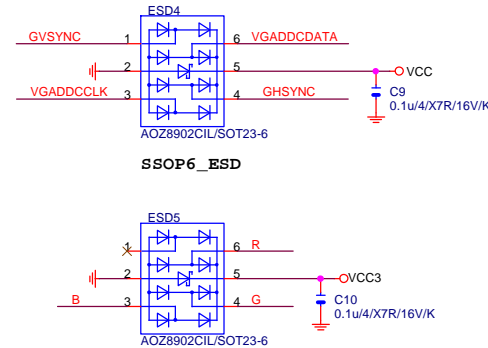
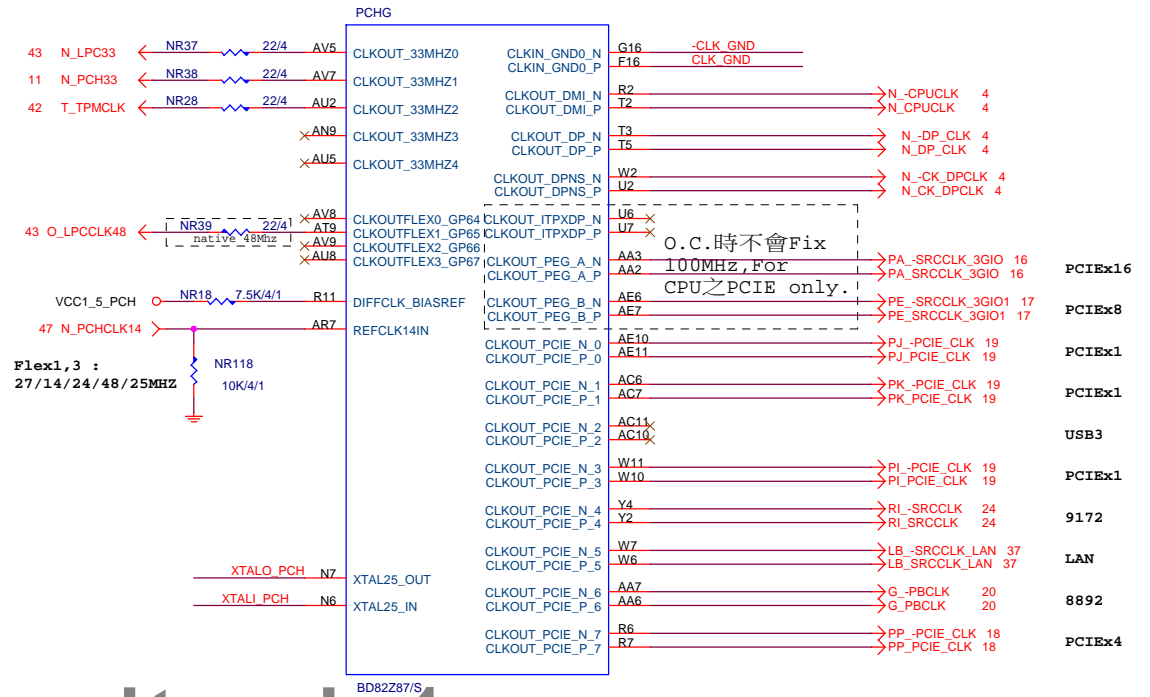
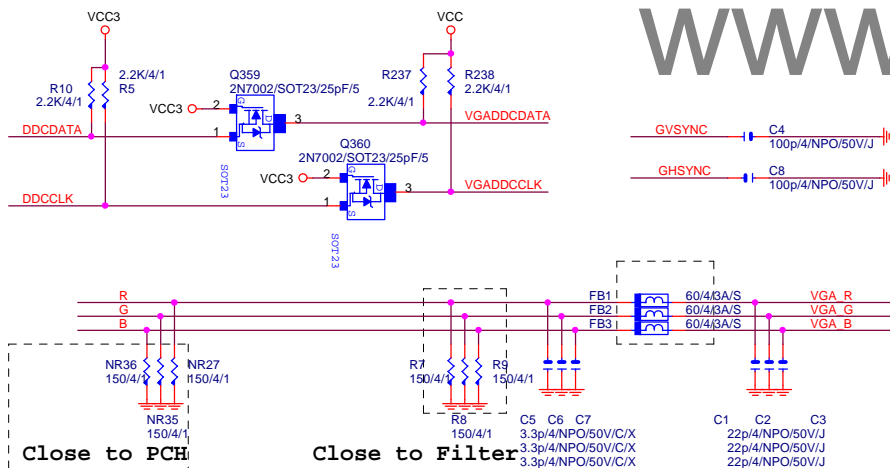
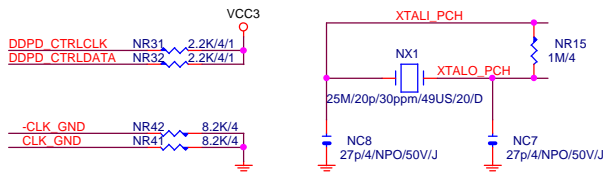
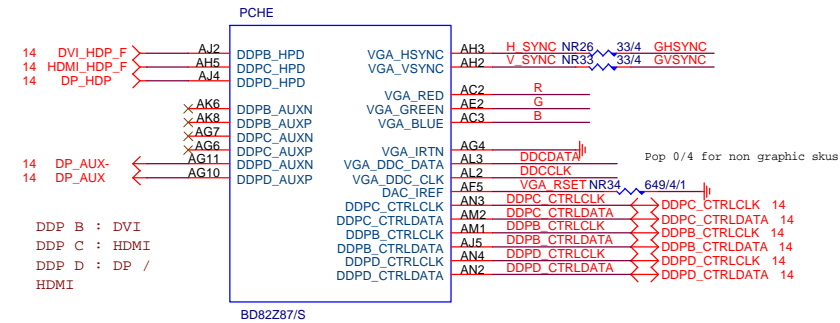
DDR3_4



Gigabyte Technology			
Title			
DDR3 CHANNEL A			
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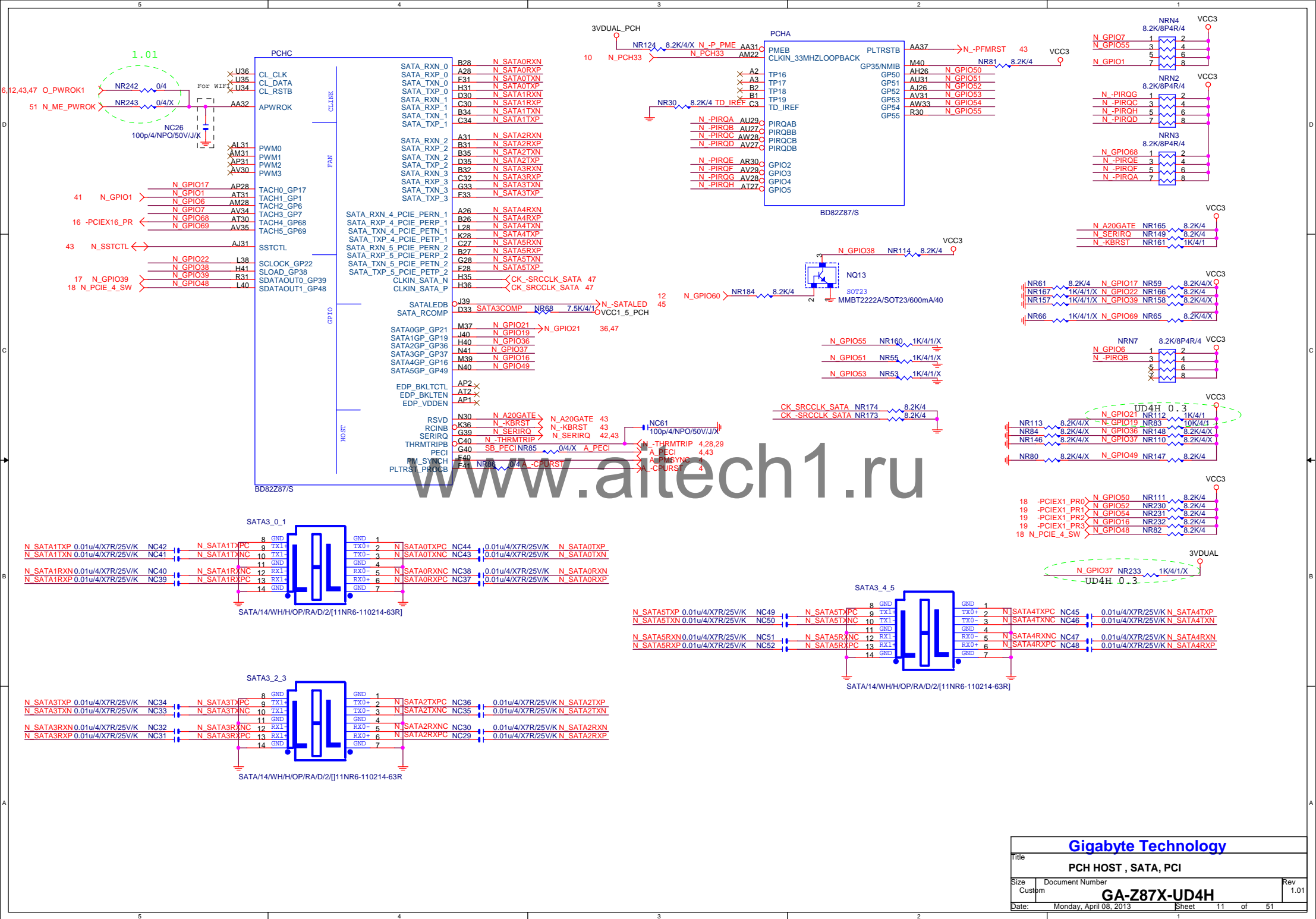


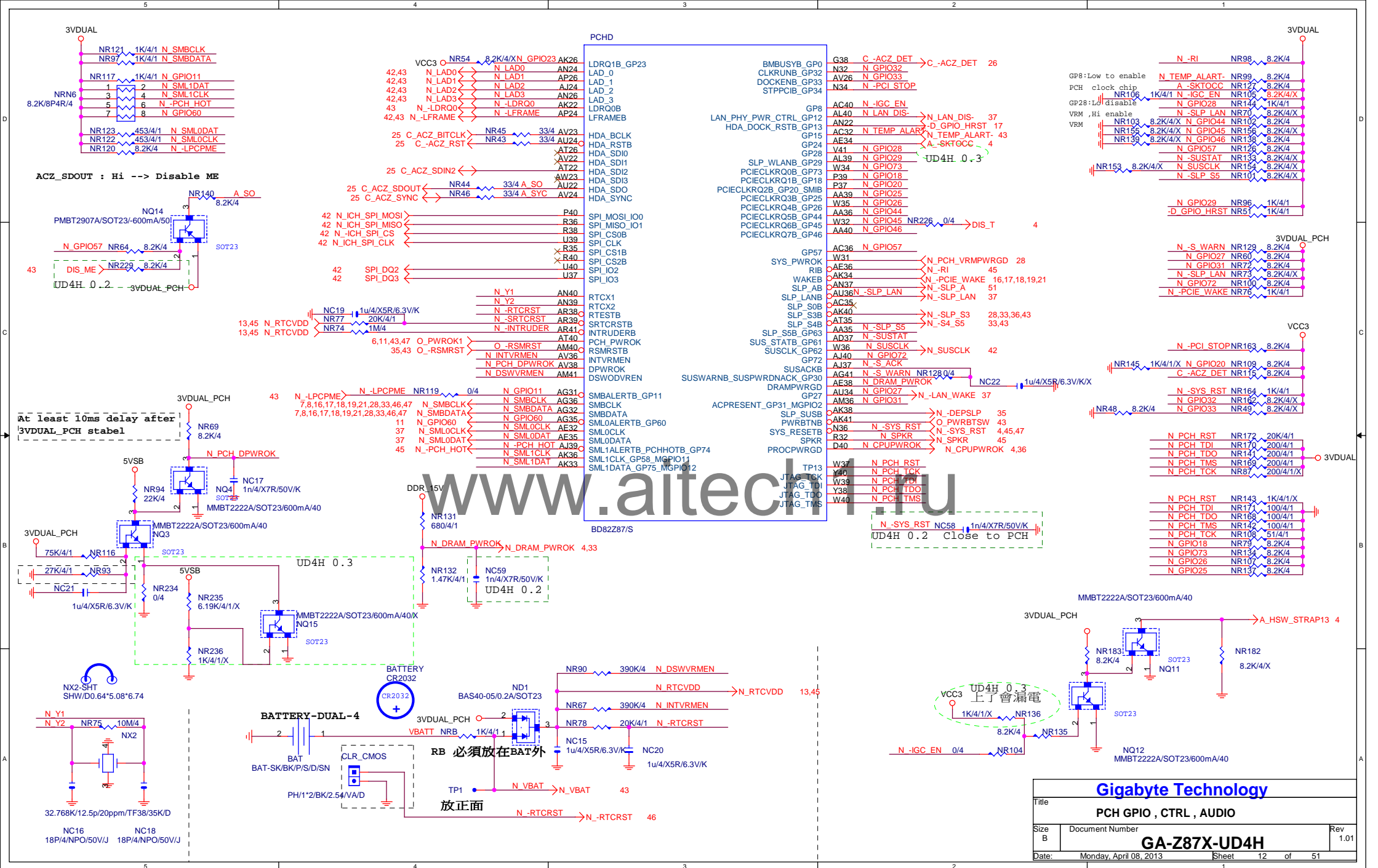


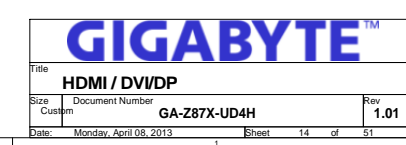
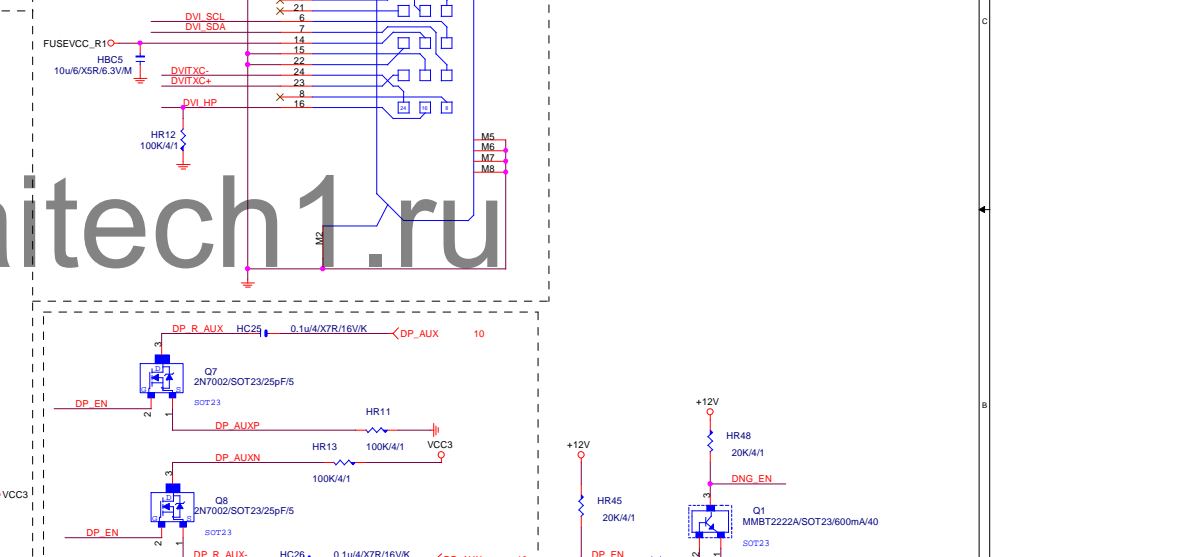
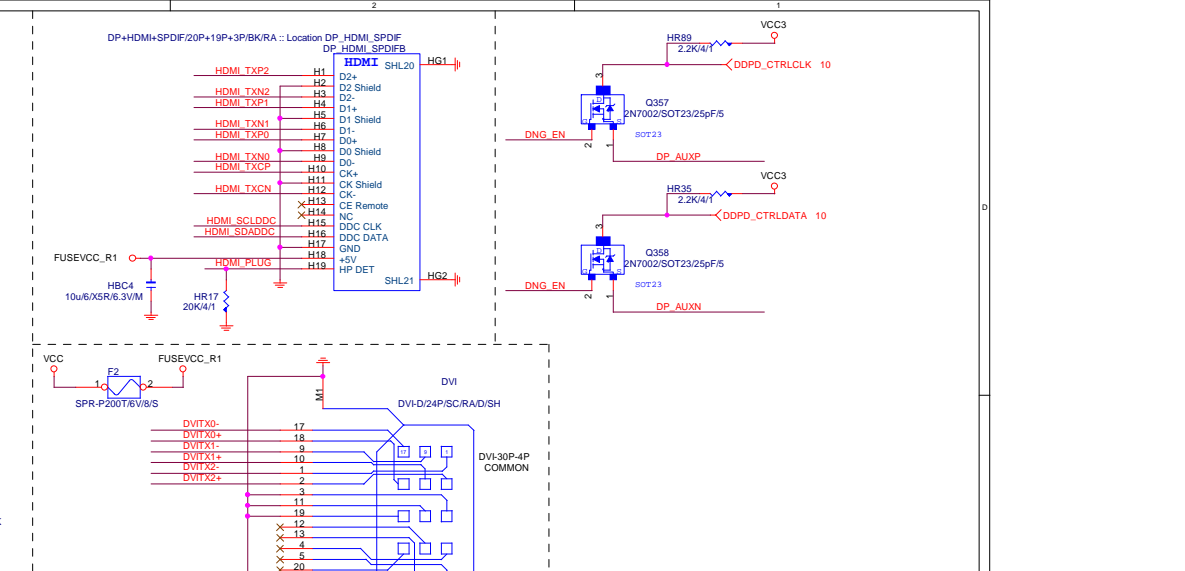


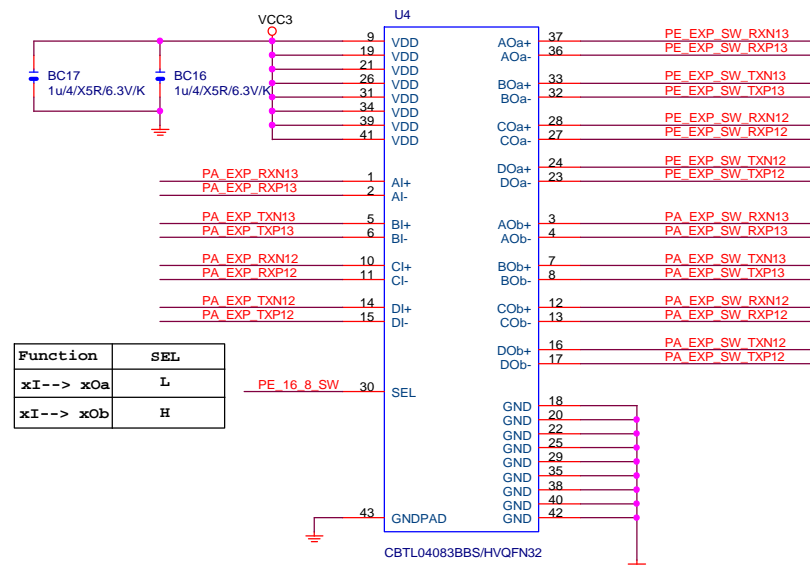
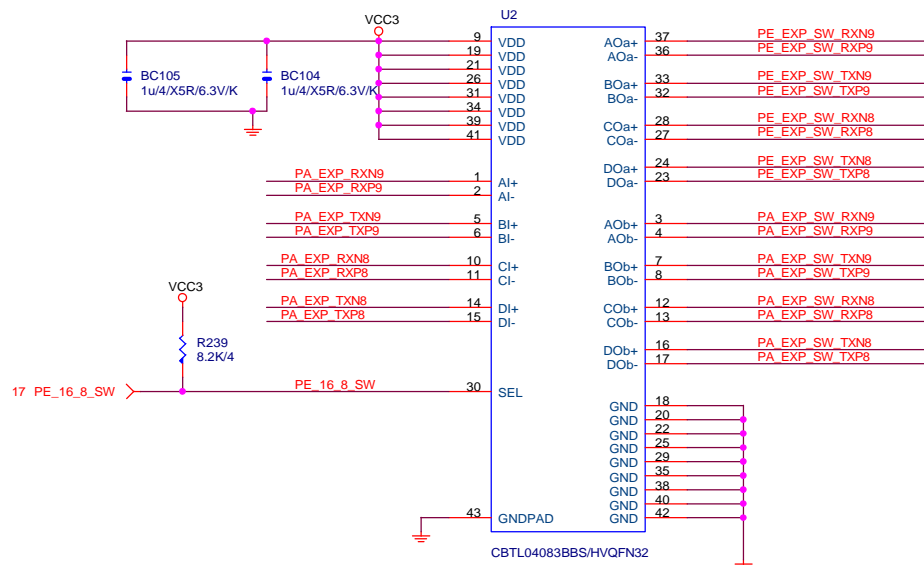
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Gigabyte Technology			
Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number		Rev
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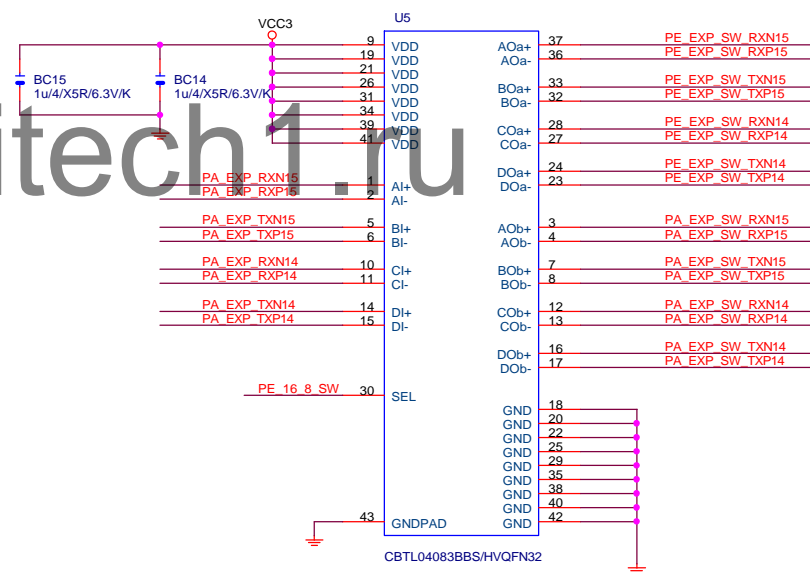
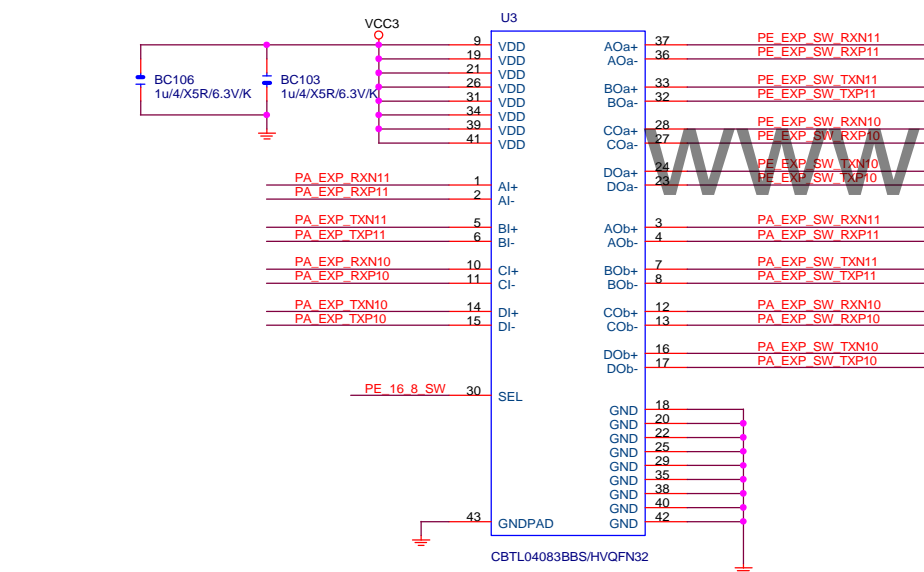




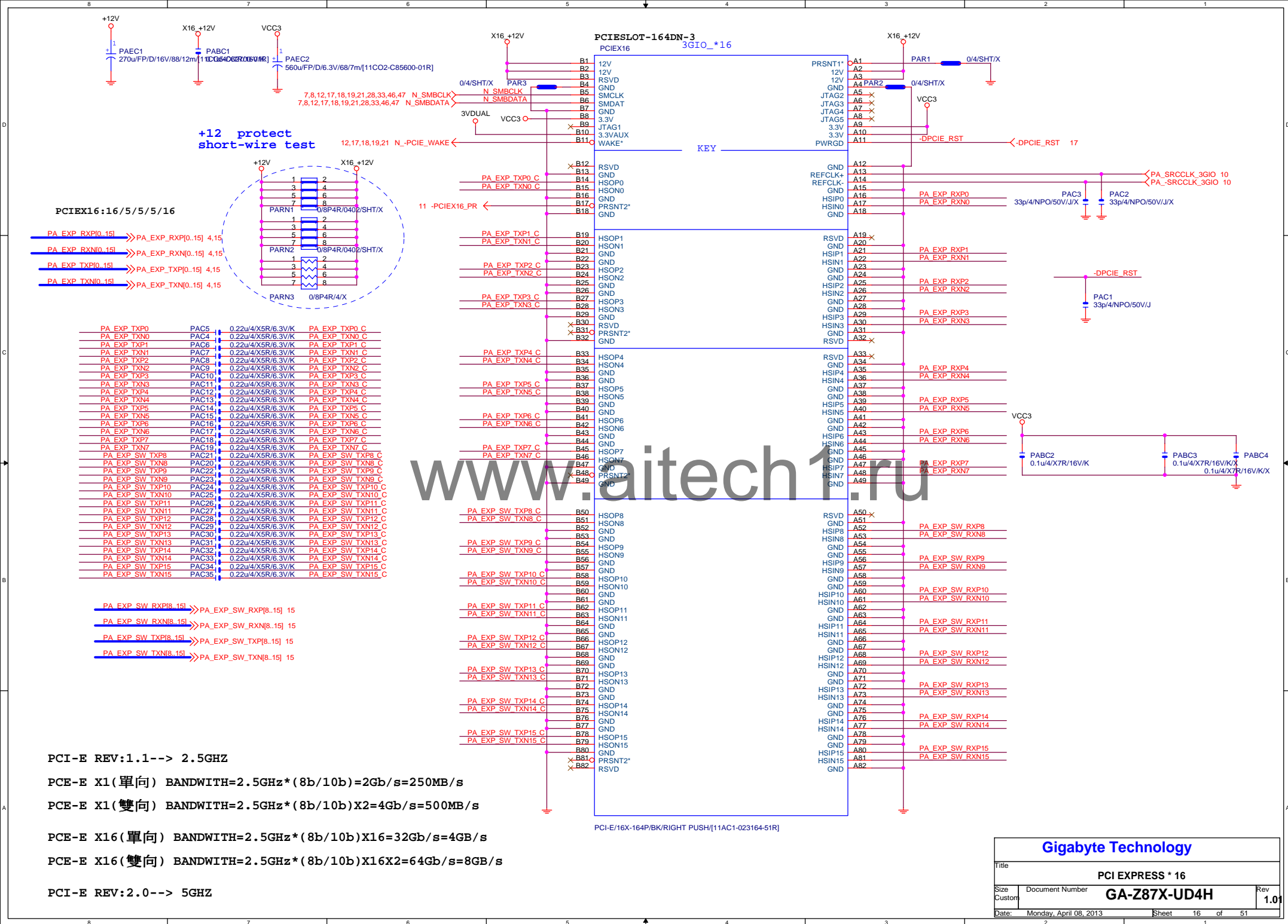




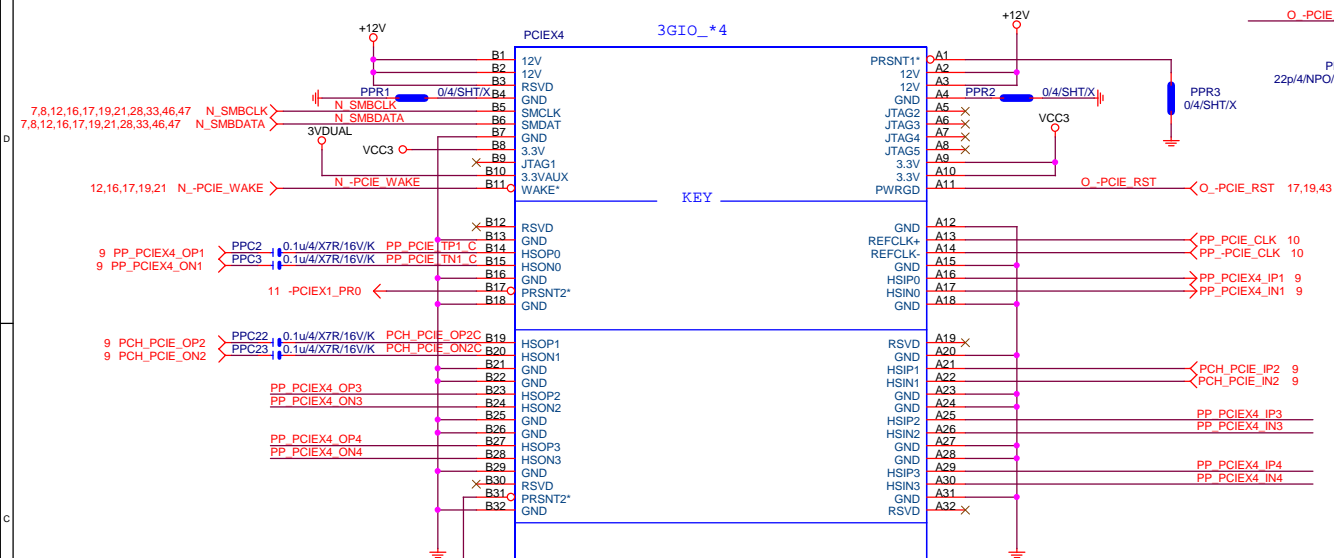
Function	SEL
xI--> xOa	L
xI--> xOb	H



PA_EXP_SW_RXP[8..15] >> PA_EXP_SW_RXP[8..15] 16	PE_EXP_SW_RXP[8..15] >> PE_EXP_SW_RXP[8..15] 17	PA_EXP_RXP[0..15] >> PA_EXP_RXP[0..15] 4,16
PA_EXP_SW_RXN[8..15] >> PA_EXP_SW_RXN[8..15] 16	PE_EXP_SW_RXN[8..15] >> PE_EXP_SW_RXN[8..15] 17	PA_EXP_RXN[0..15] >> PA_EXP_RXN[0..15] 4,16
PA_EXP_SW_TXP[8..15] >> PA_EXP_SW_TXP[8..15] 16	PE_EXP_SW_TXP[8..15] >> PE_EXP_SW_TXP[8..15] 17	PA_EXP_TXP[0..15] >> PA_EXP_TXP[0..15] 4,16
PA_EXP_SW_TXN[8..15] >> PA_EXP_SW_TXN[8..15] 16	PE_EXP_SW_TXN[8..15] >> PE_EXP_SW_TXN[8..15] 17	PA_EXP_TXN[0..15] >> PA_EXP_TXN[0..15] 4,16



PCIE*4

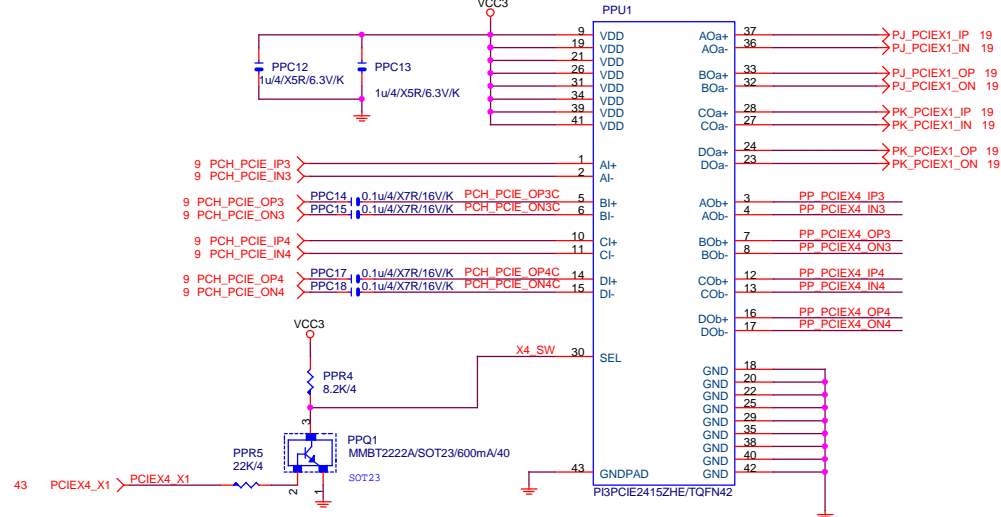
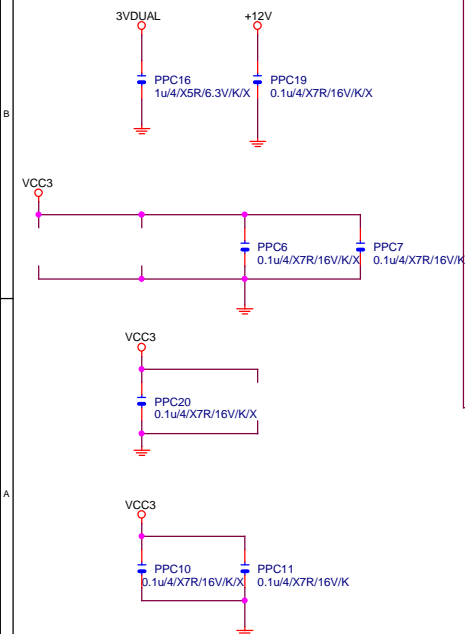


BIOS只偵測此pin(GPIO48)

Lo: 設為1個x4
Hi: 設為4個x1

HI 又為4回X1

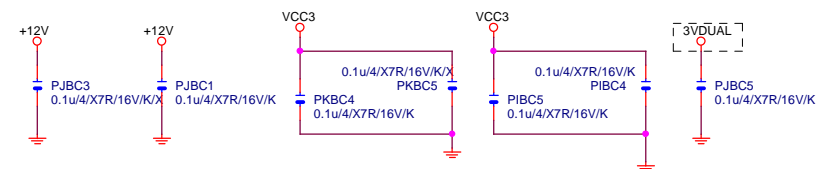
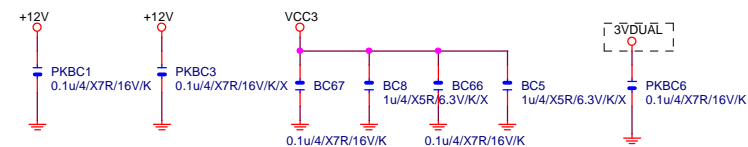
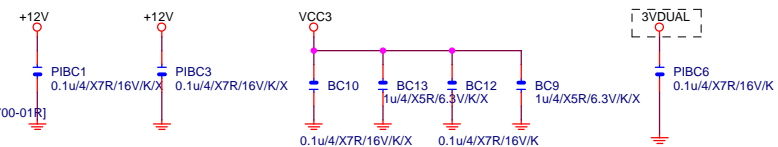
通知BIOS DETECTED DEVICE

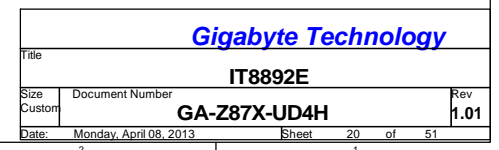


Function	SEL
xI--> x0a	L;PCIEX4 SLOT-->X
xI--> x0b	H;PCIEX4 SLOT-->X

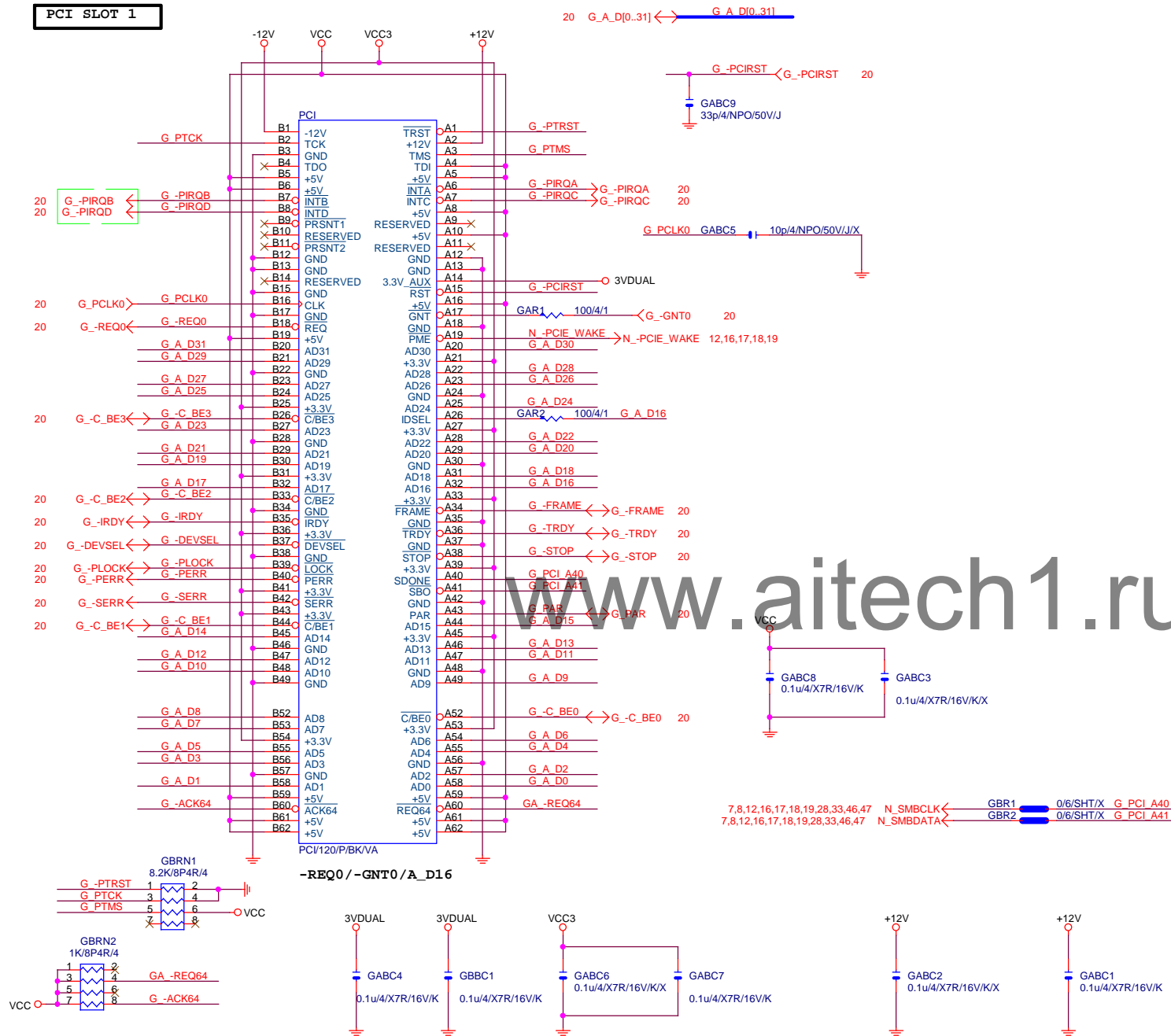


Title			
PCIE_X4			
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PCI SLOT 1



GIGABYTE™

Title
PCI SLOT 1&2

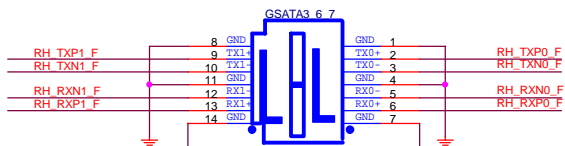
Size B Document Number

GA-Z87X-UD4H

Rev
1.01

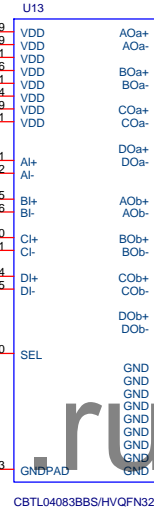
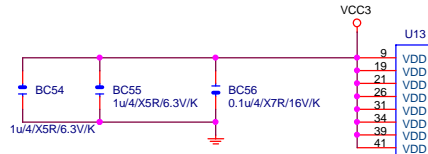
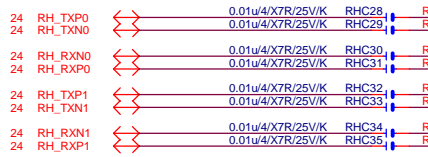
Date: Monday, April 08, 2013

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SATA14/GR/H/OP/RA/D/2
GRAY connector for SATA3

90欧姆:[15/4.5/7.5/4.5/15]

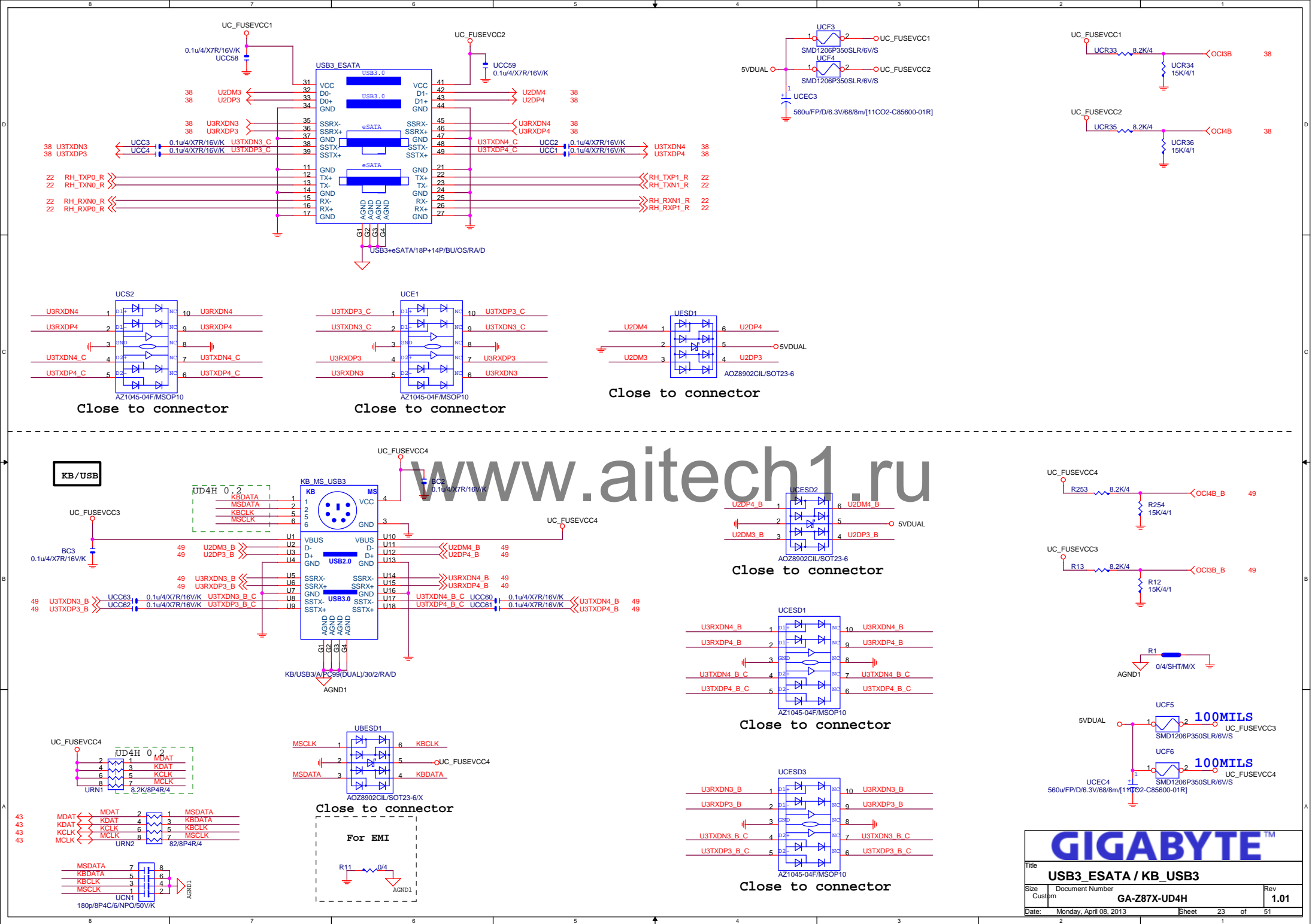


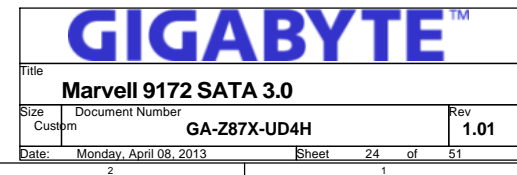
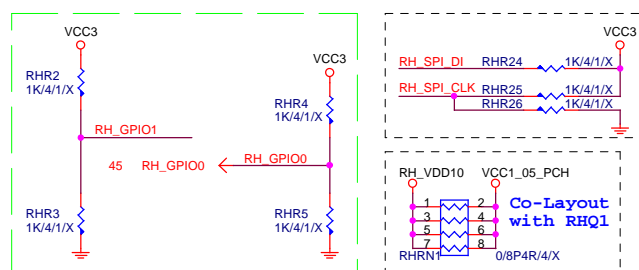
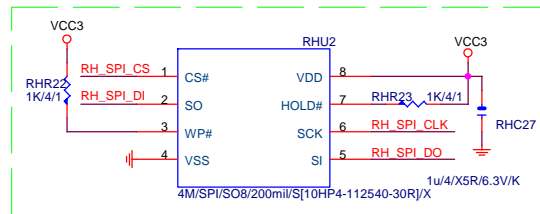
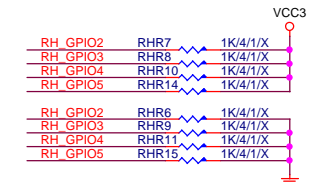
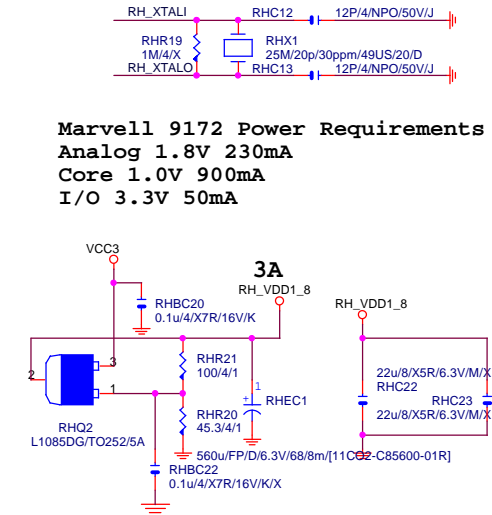
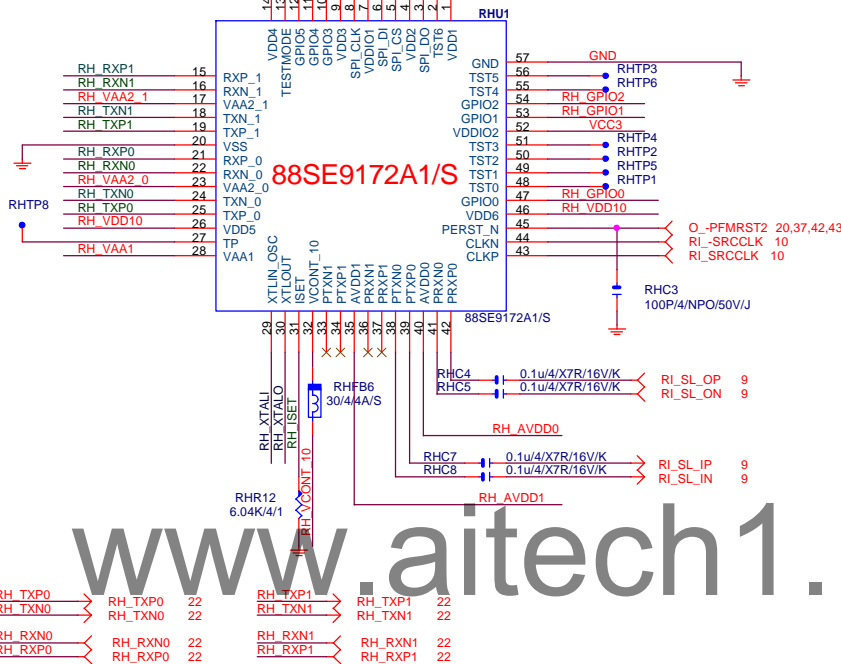
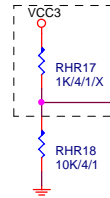
eSATA

Front
SATA

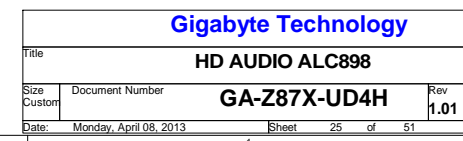
Function	SEL
xI--> xOa	L
xI--> xOb	H

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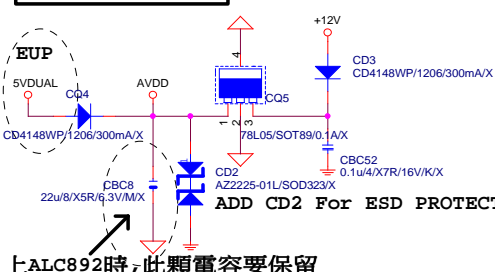




JD resistors close to pin34 of CODEC

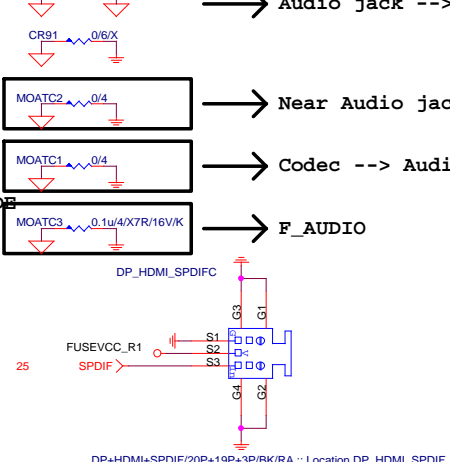


CODEC POWER/EMI PAD



上ALC892時,此顆電容要保留

Audio jack --> USB



LINE-OUT

Near Audio jack left

Codec --> Audio jack

F_AUDIO

LINE-IN

MIC-IN

SURROUND

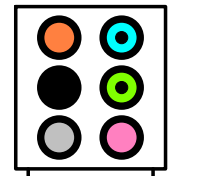
CEN/LFE

SURRBACK

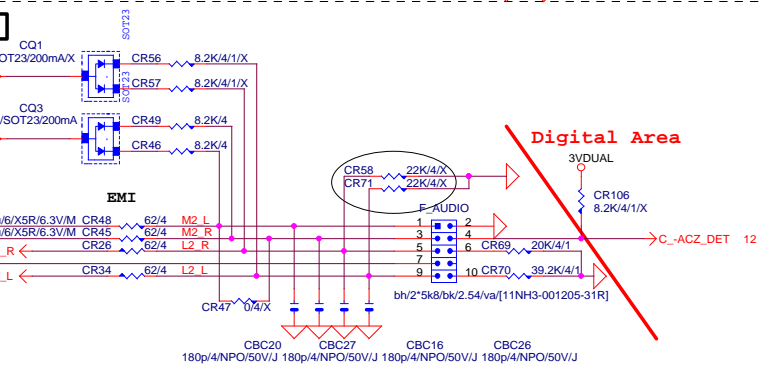
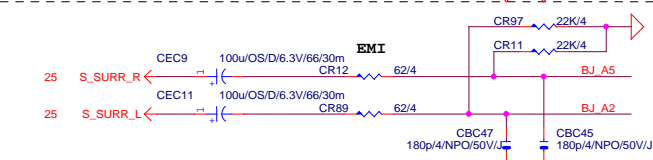
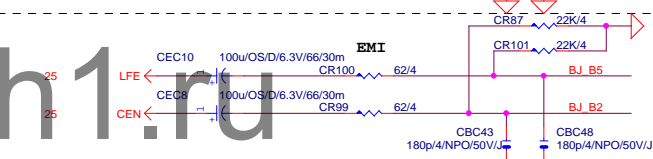
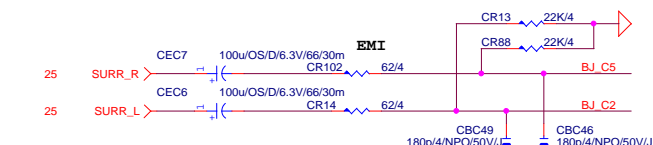
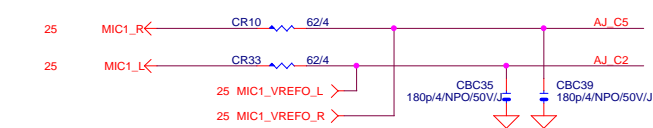
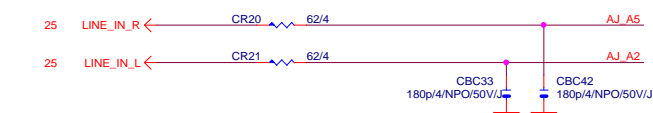
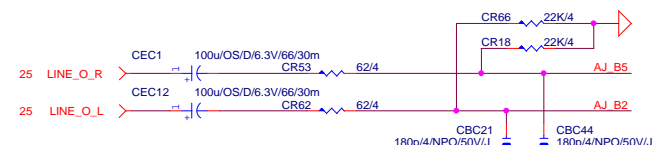
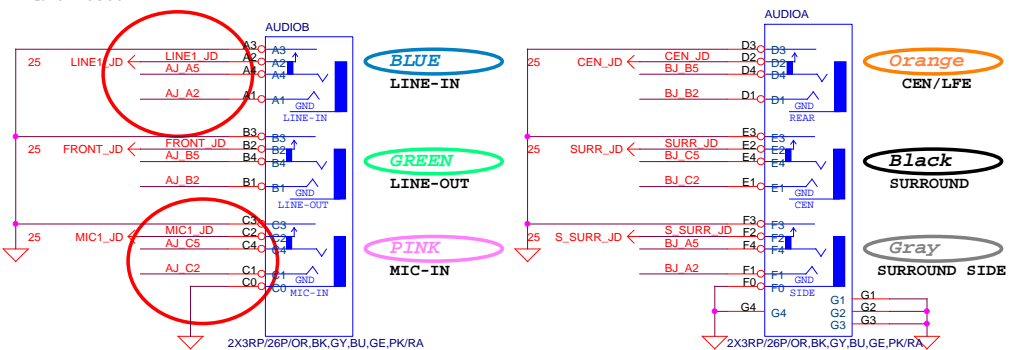
AZALIA FRONT PANEL

AZALIA JACK

BTX AZALIA CONNECTOR



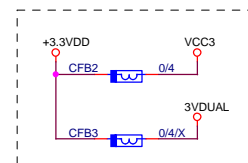
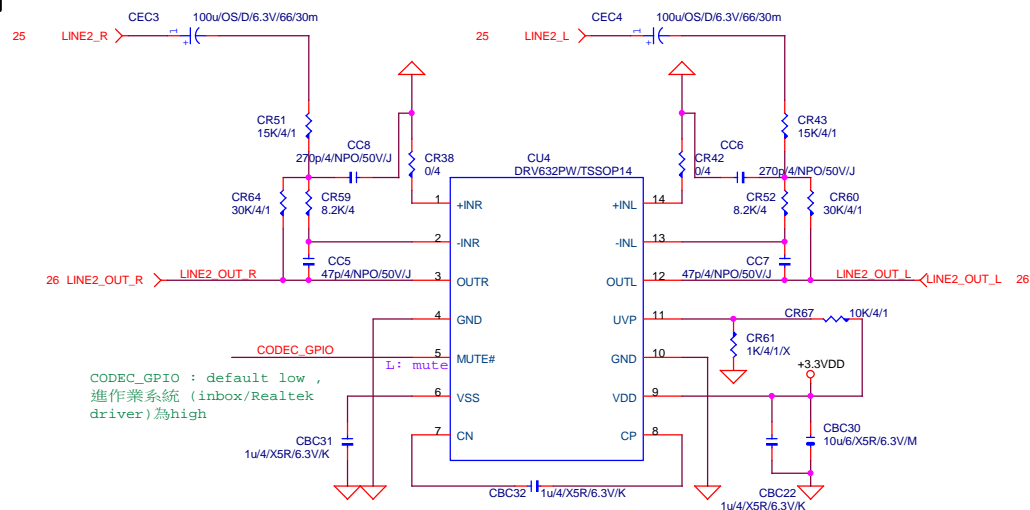
11NR6-403007-21R



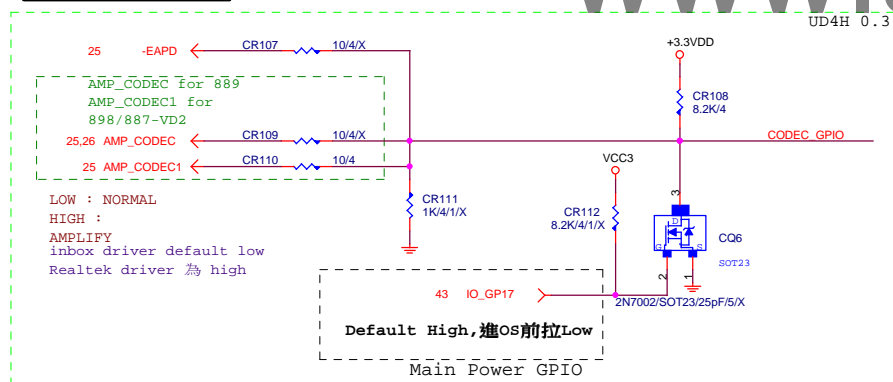
Digital Area

Gigabyte Technology			
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AUDIO JACK			
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HEADPHONE



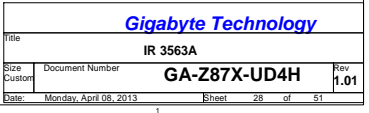
For Pop Noise

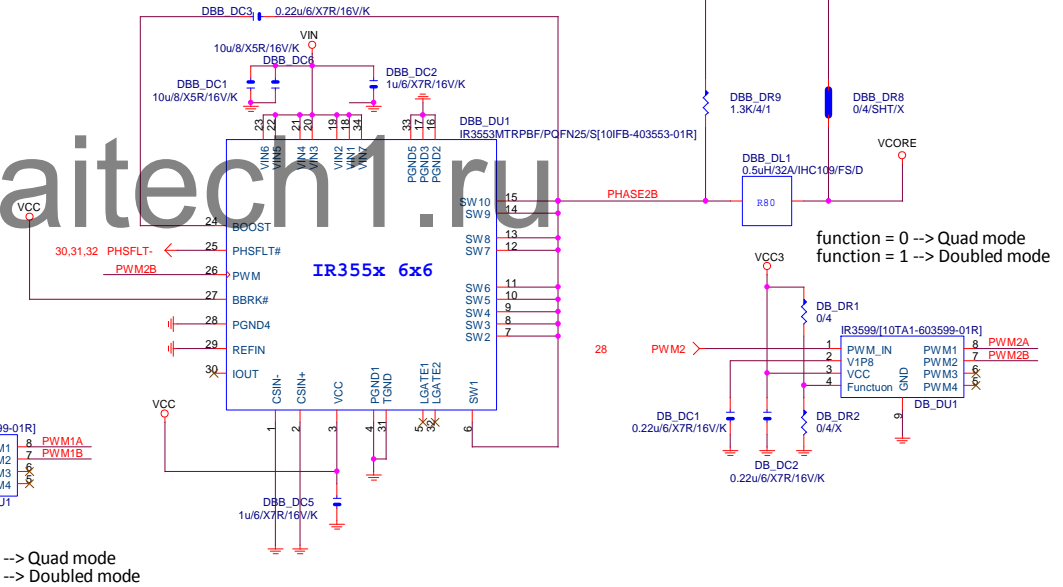
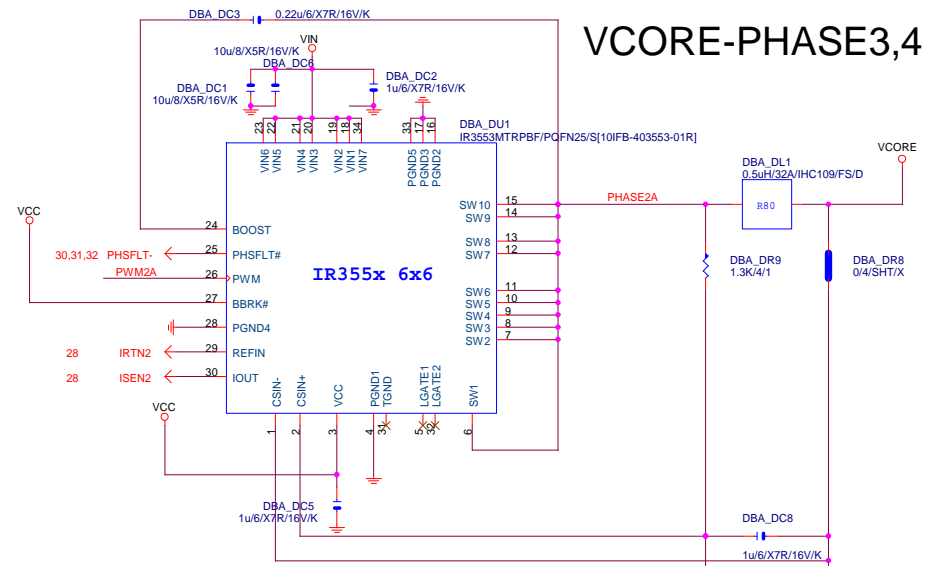
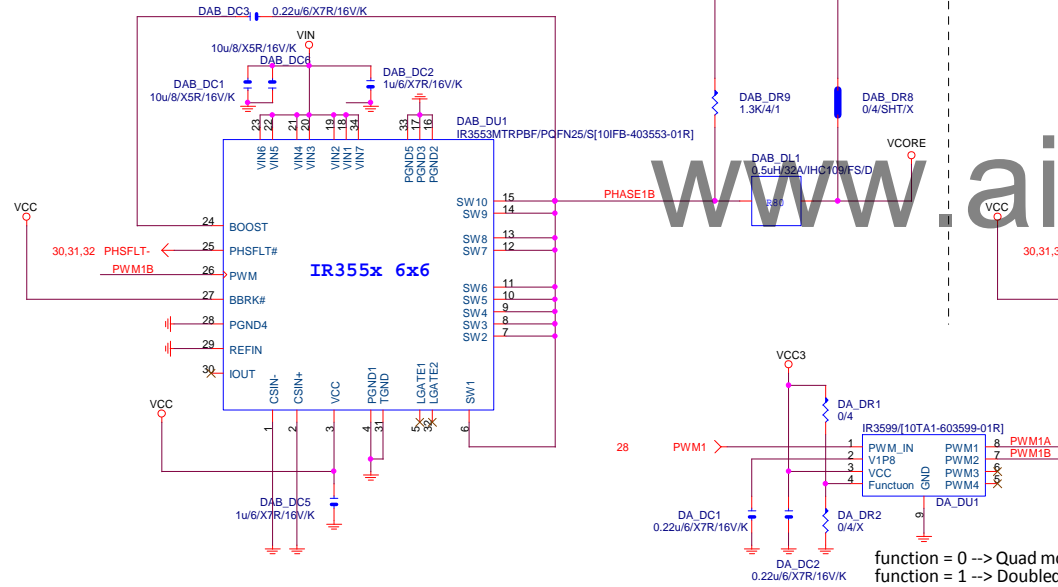
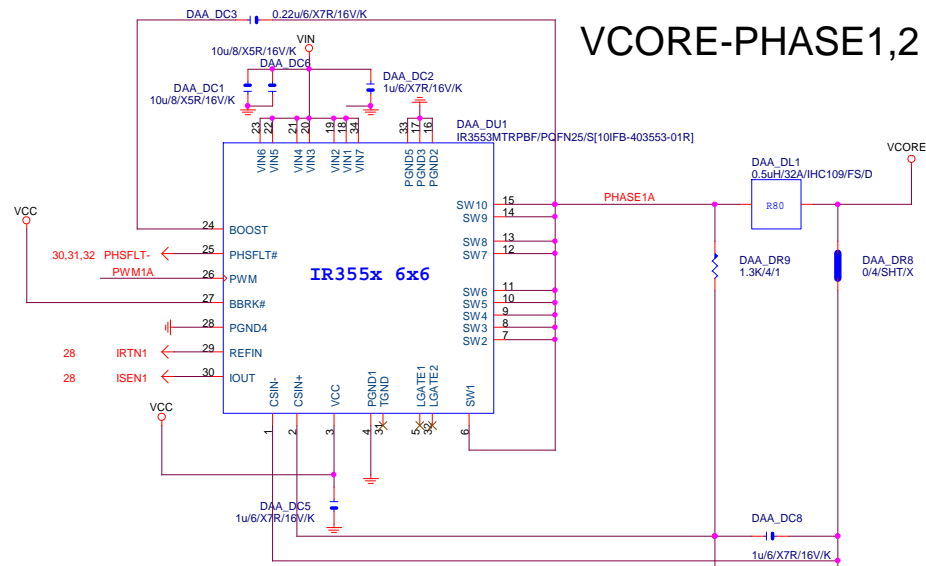


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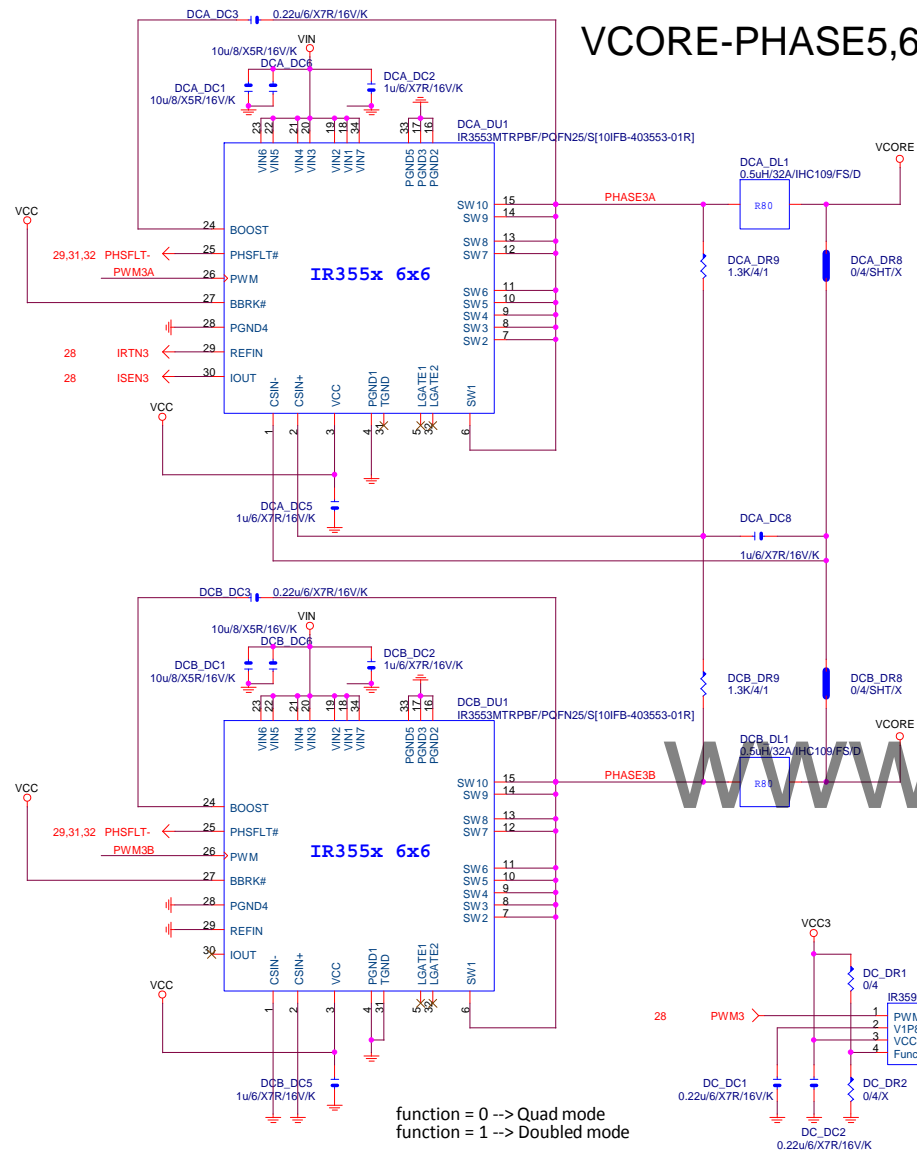
Title			
8-CH DAC & Anti-Pop / Mute			
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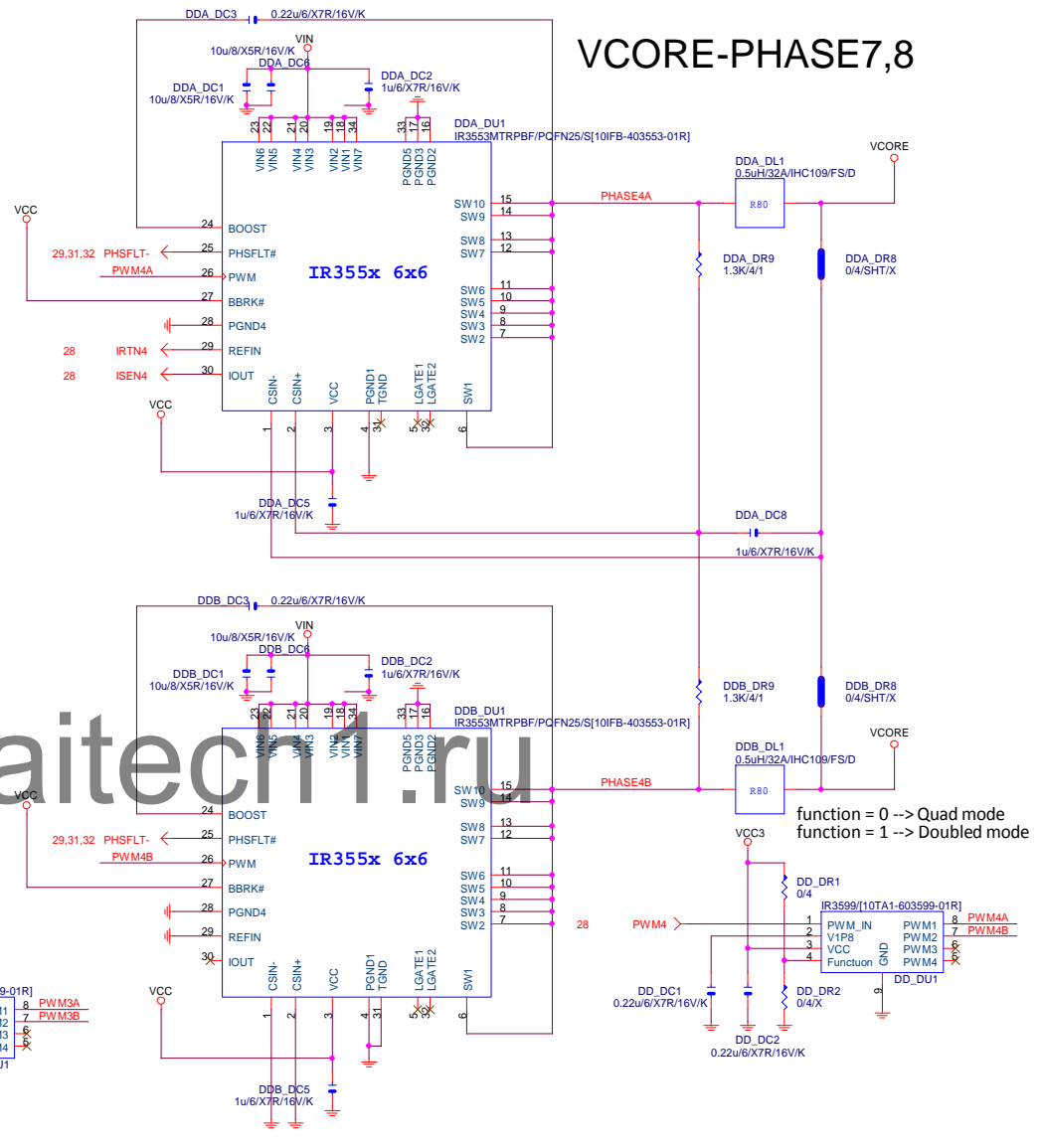


Add MOSFET Anti-Burn
4.11.28 N_THRMTRIP <-- DAR109 0/4 PHSFLT- UD4H 0.3 VCC
6.2K/4/X

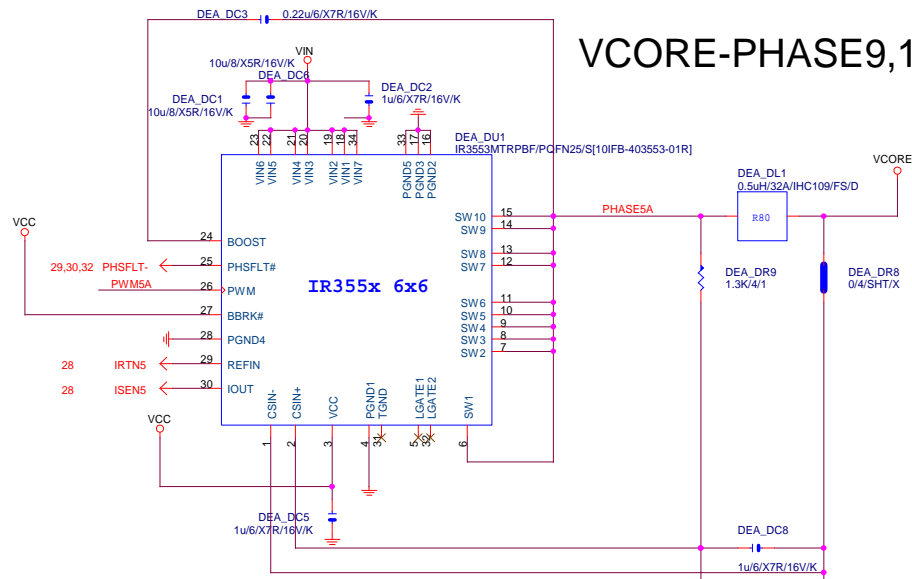
VCORE-PHASE5,6



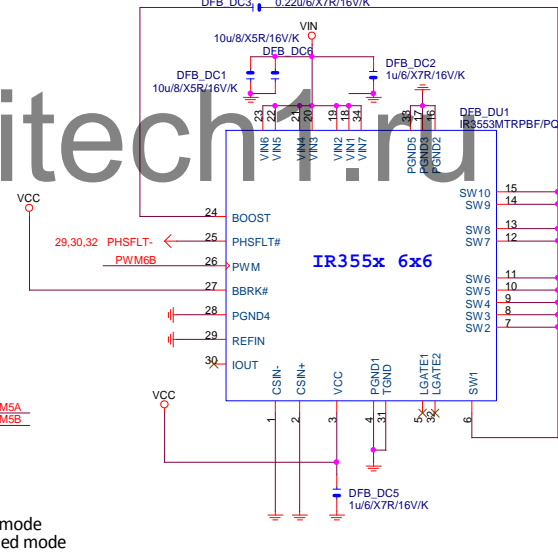
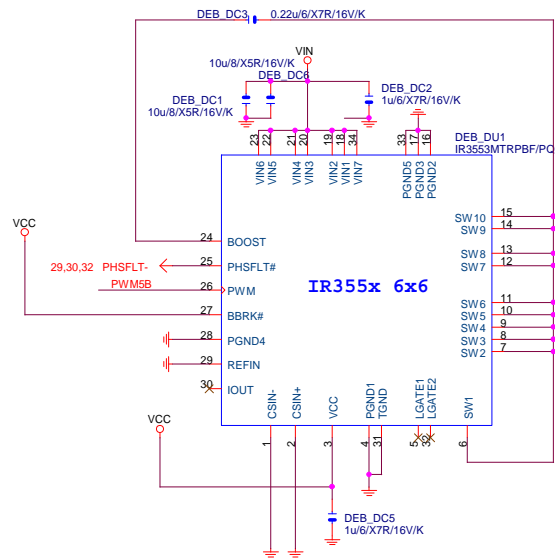
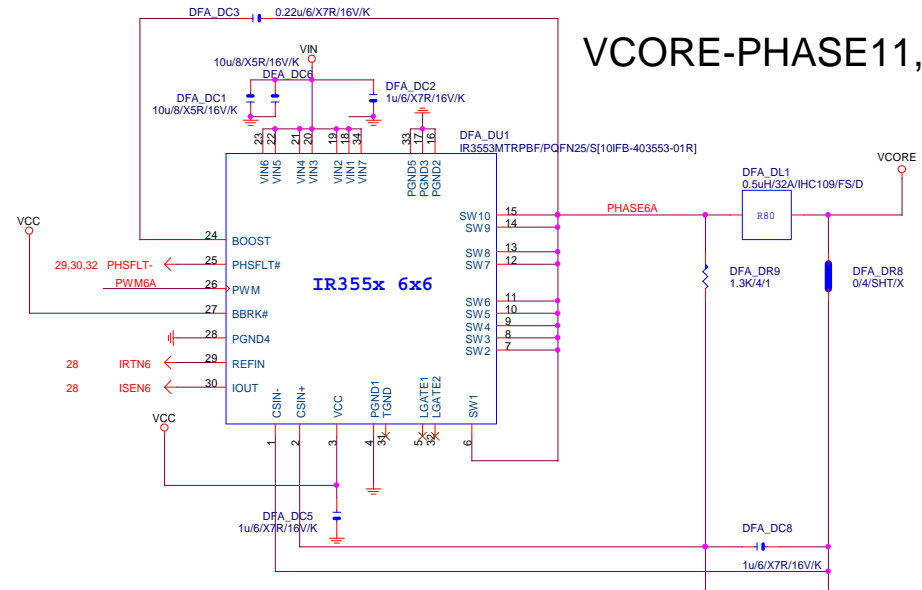
VCORE-PHASE7,8



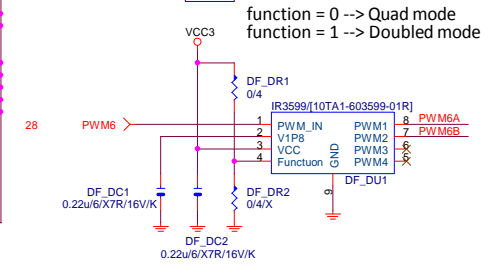
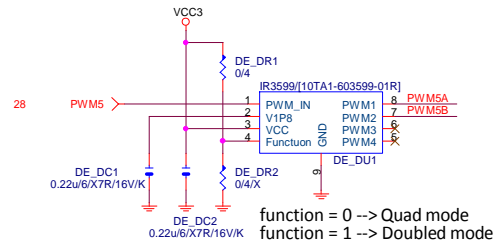
VCORE-PHASE9,10



VCORE-PHASE11,12



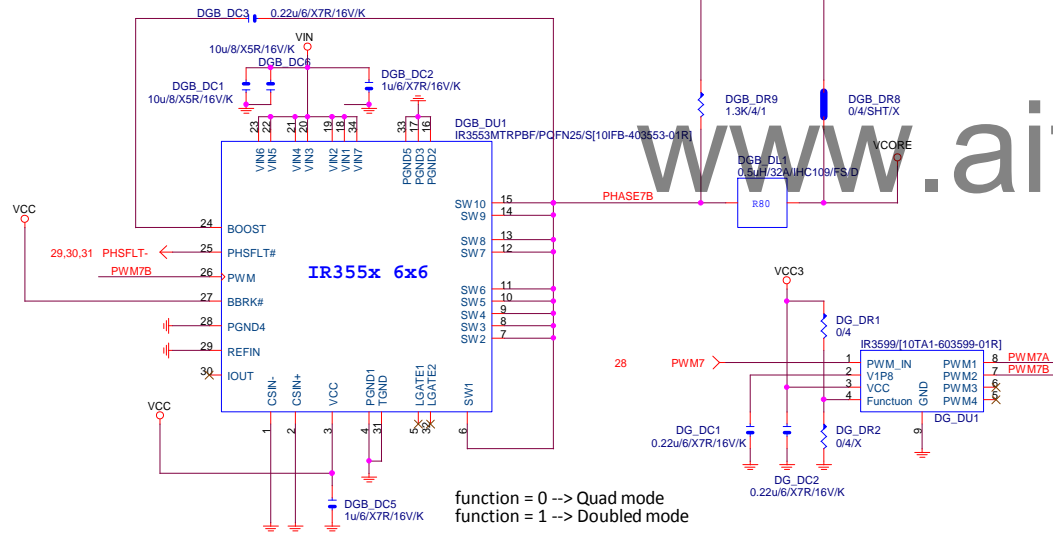
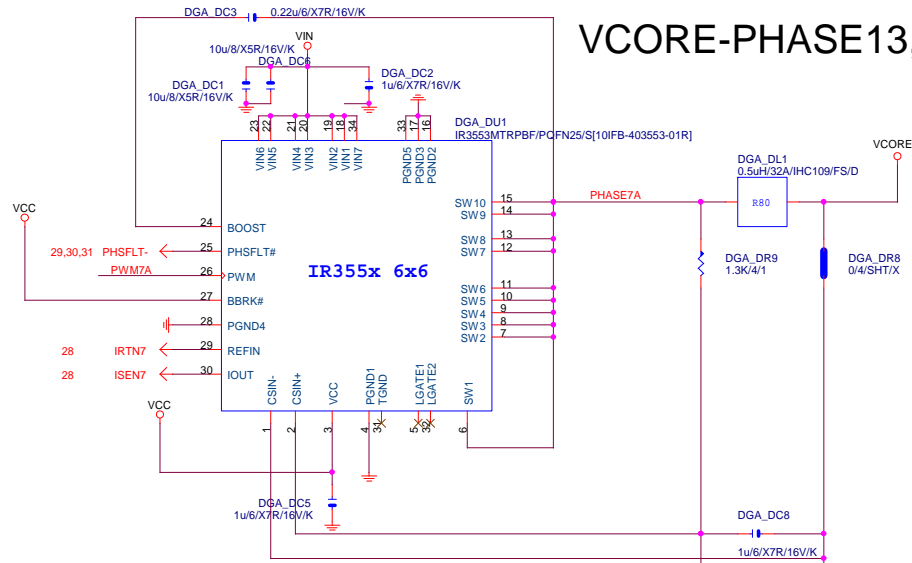
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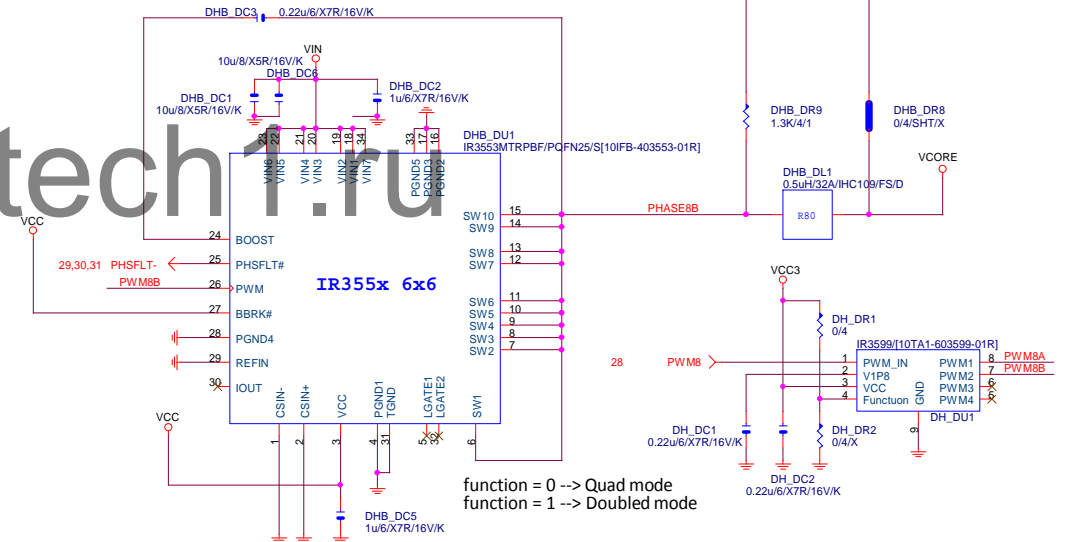
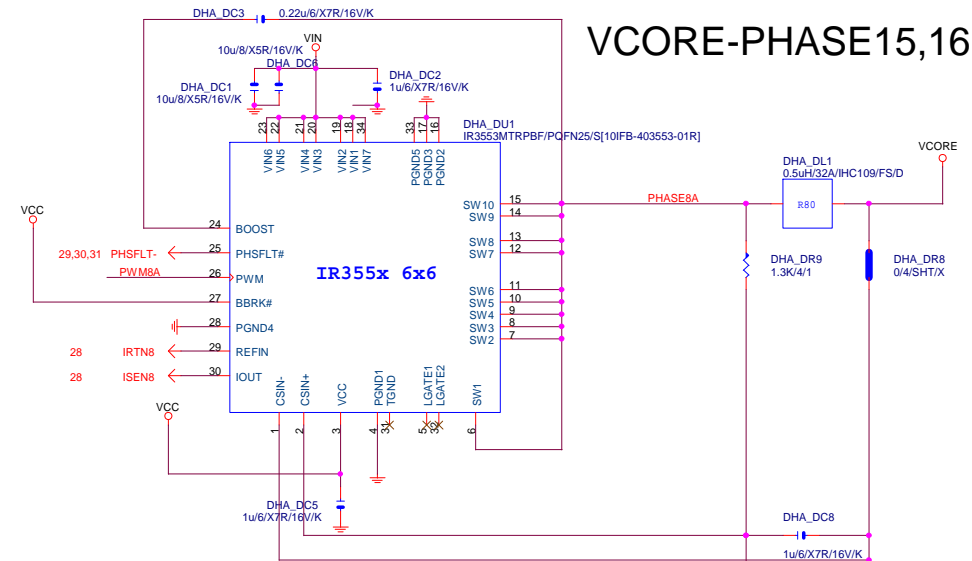
function = 0 --> Quad mode
function = 1 --> Doubled mode

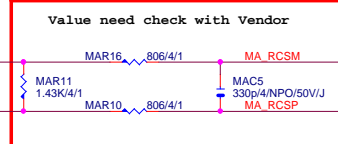
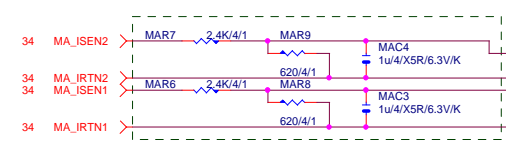
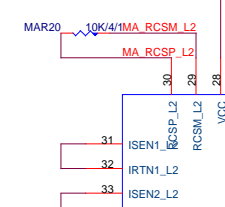
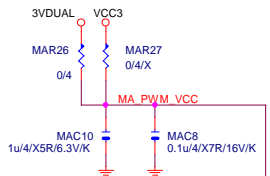
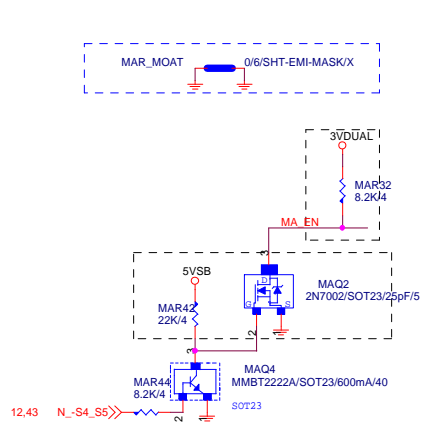
Gigabyte Technology			
Title			
IR3553-VCORE			
Size	Document Number	GA-Z87X-UD4H	
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VCORE-PHASE13,14



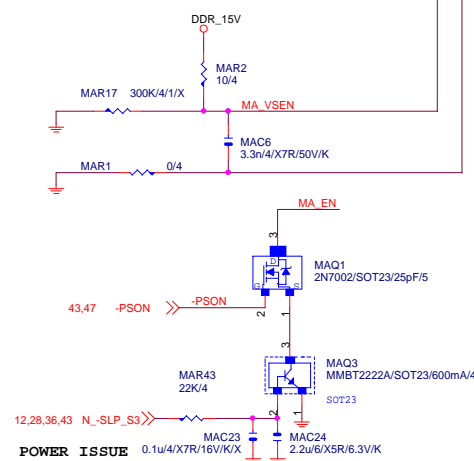
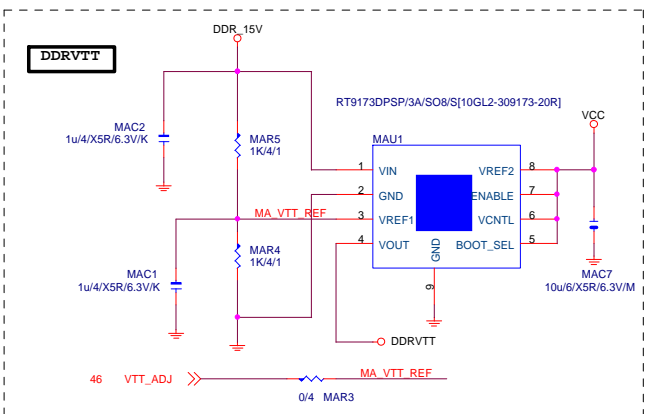
VCORE-PHASE15,16





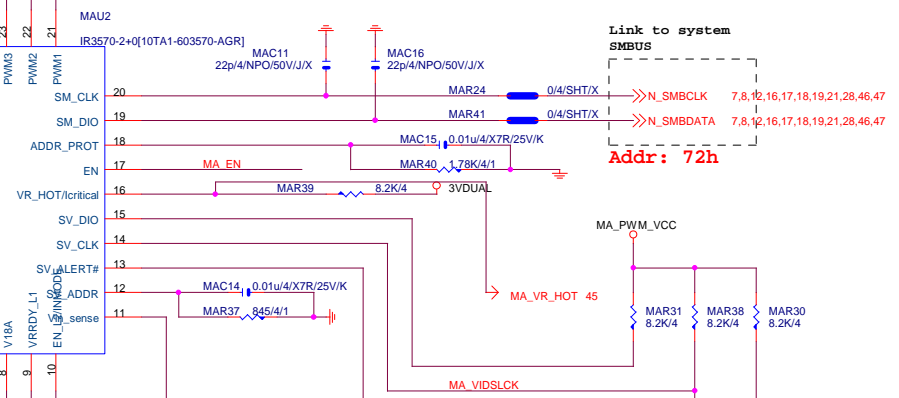
Close to DDR
output
inductor

should be routed as
differential pair,
7mil width, 8mil
spacing



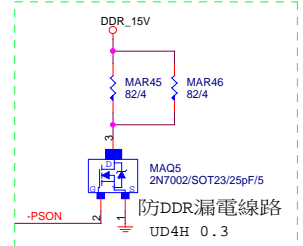
POWER ISSUE 0.1uF/4X7R/16V/K

IR3570



Link to system
SMBUS
Addr: 72h

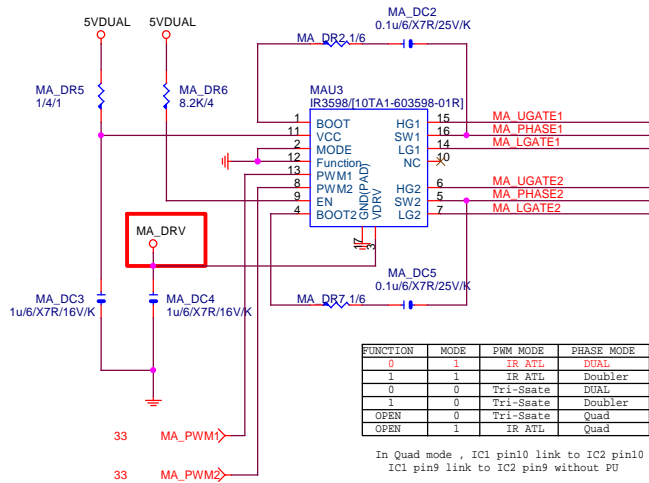
Link to PCH
pin BG46
Pull up in PCH side



防DDR漏電線路
UD4H 0.3

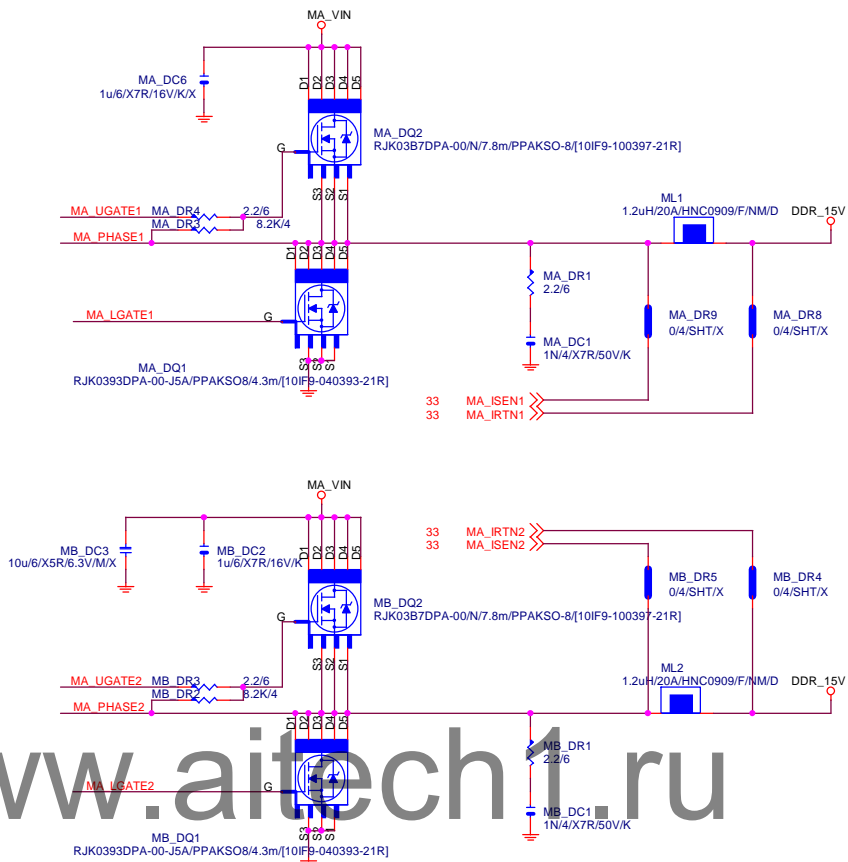
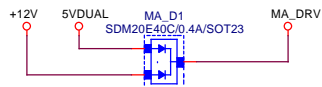
GIGABYTE™			
Title			
DDR POWER IR3570			
Size	Document Number	Rev	
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DDR_15V

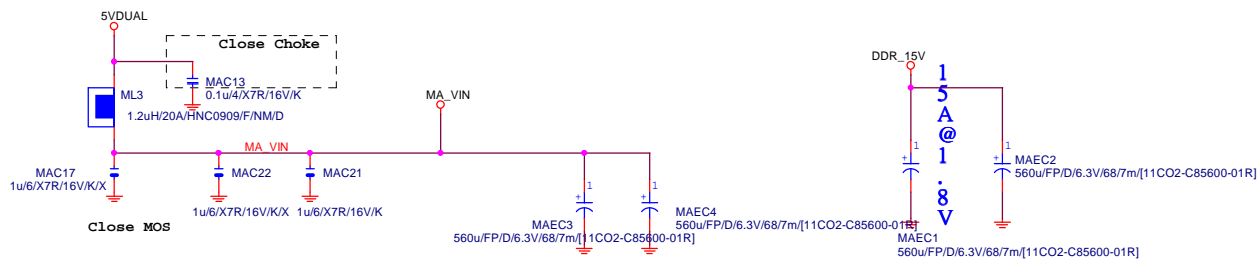


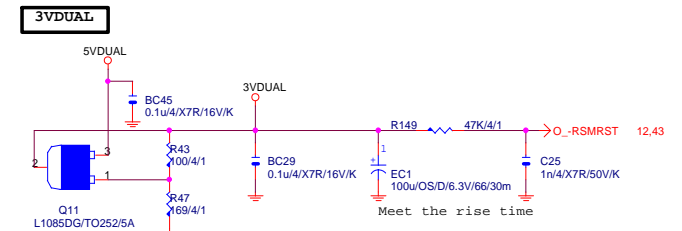
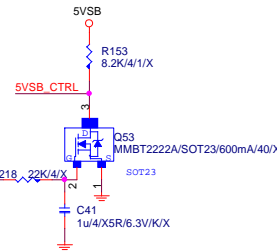
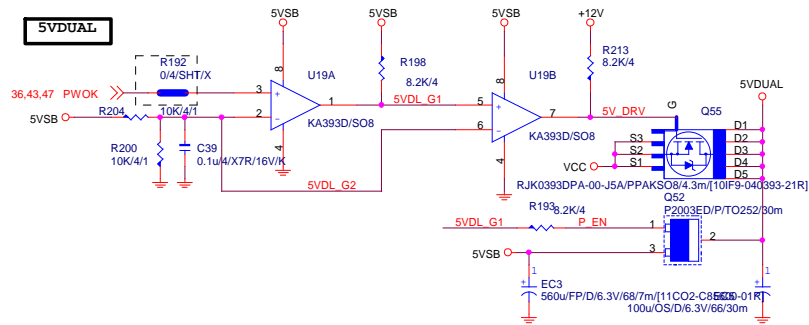
FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Saate	DUAL
1	0	Tri-Saate	Doubler
OPEN	0	Tri-Saate	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

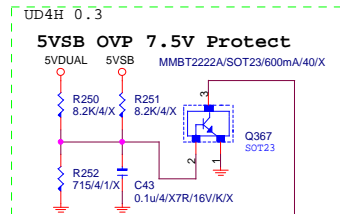
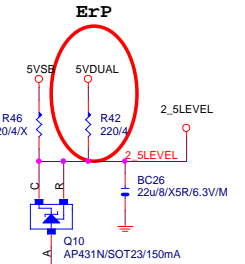
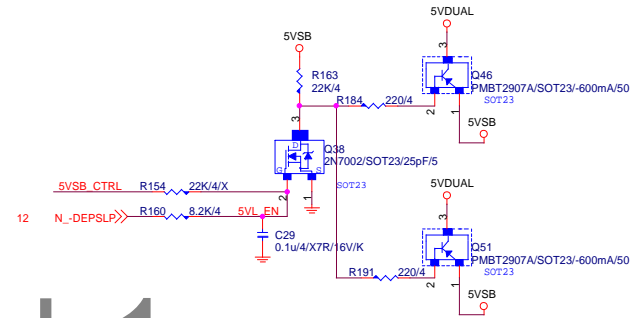
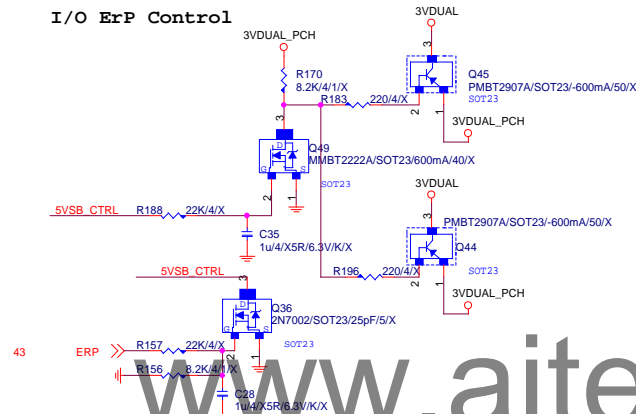


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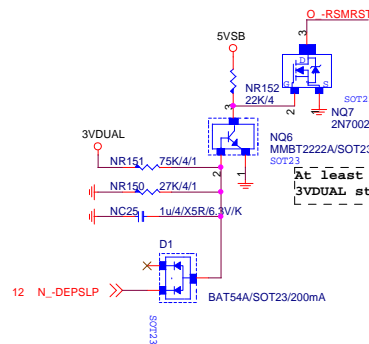
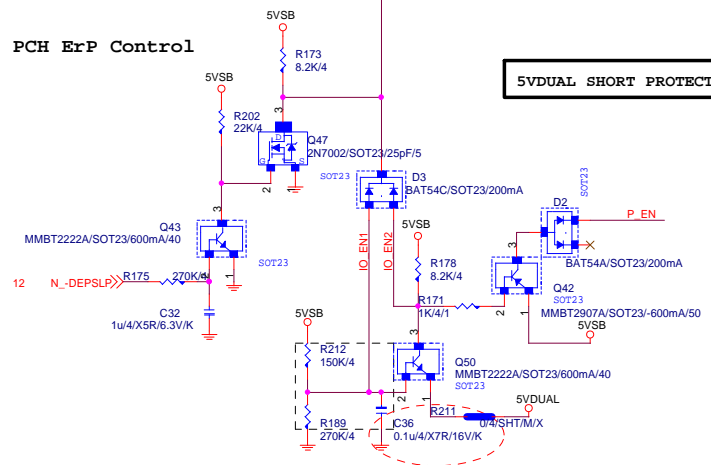




I/O ErP Control



PCH ErP Control



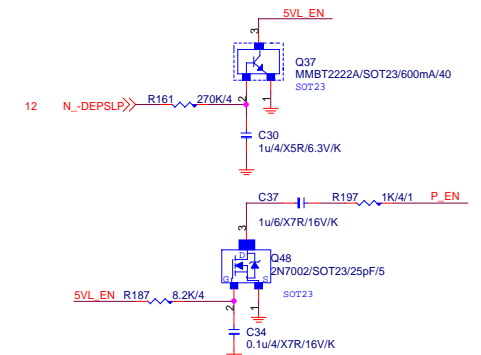
At least 10ms delay after 3VDUAL ready
Pop when PCH & SIO both use 3VDUAL-PCH

Rise/Fall max 50us

Rise:20% - 80%

Fall :2V- 0.8V

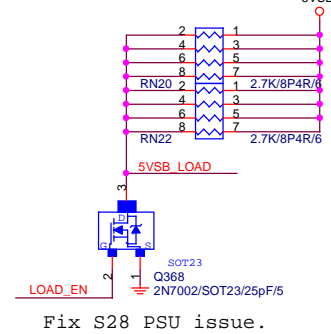
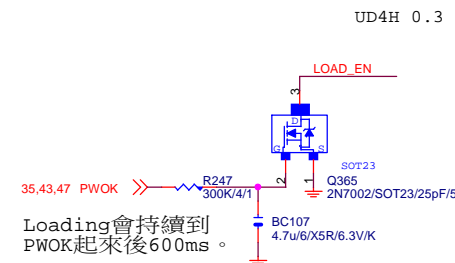
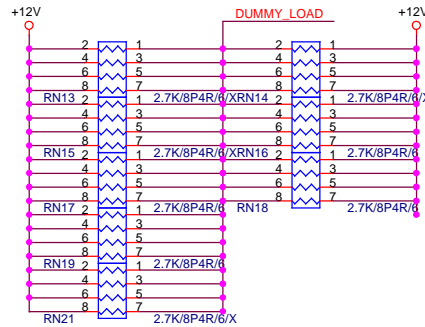
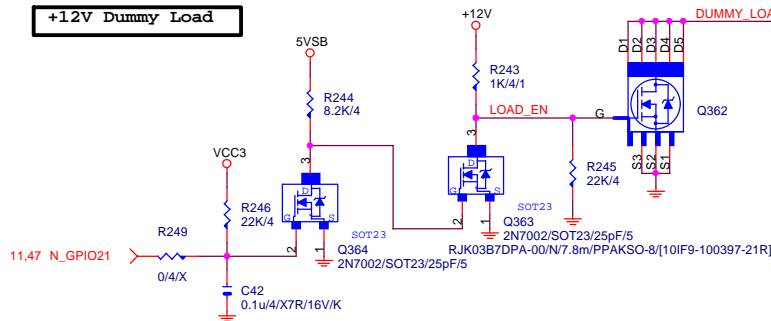
At least 10ms delay after
3VDUAL stabel



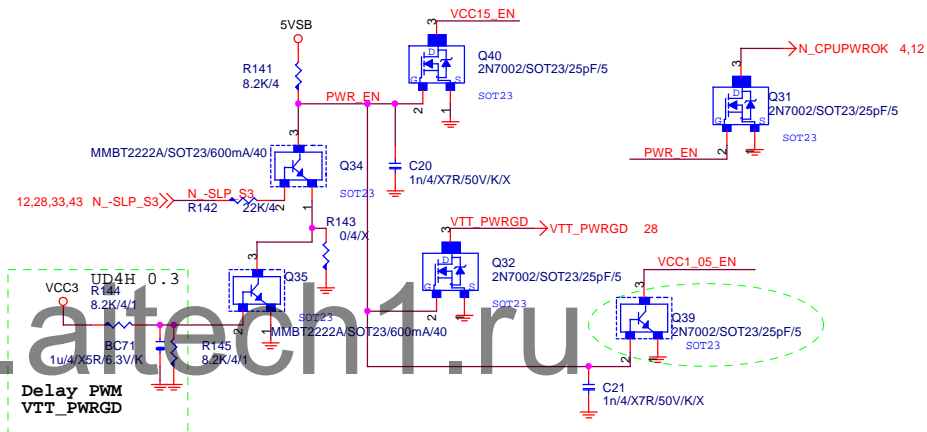
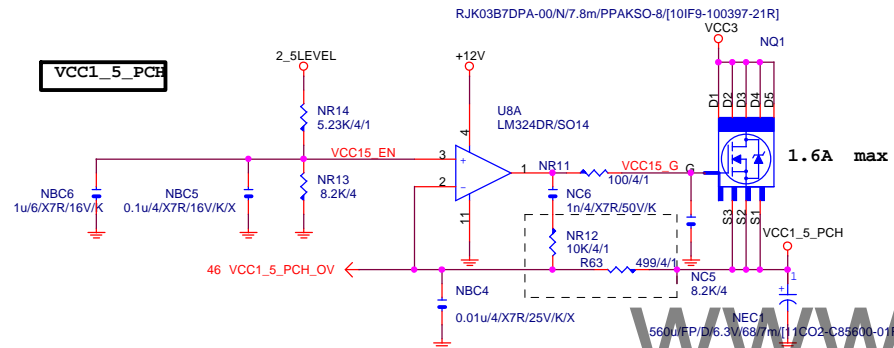
Gigabyte Technology

Title			DISCRETE POWER 1
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Custom		Rev 1.01	
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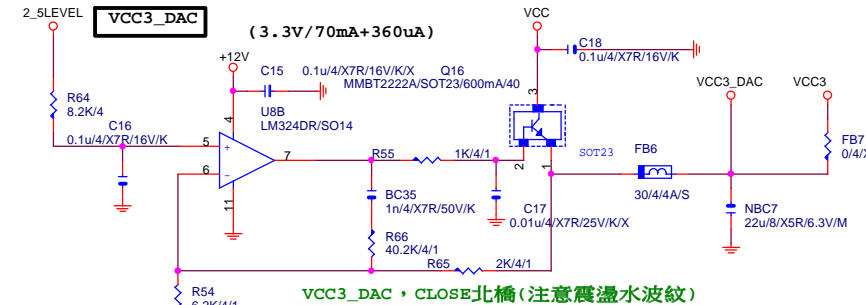
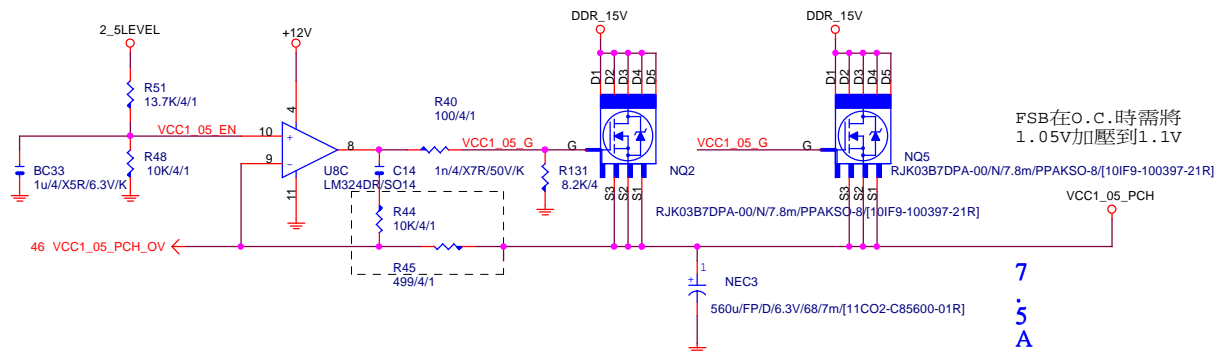
+12V Dummy Load



VCC1_5_PCH



VCC1_05_PCH

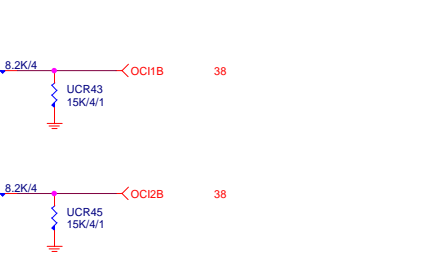
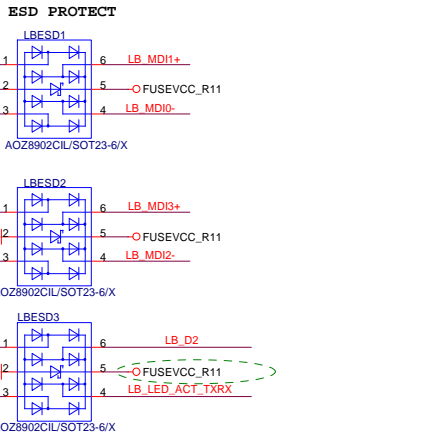
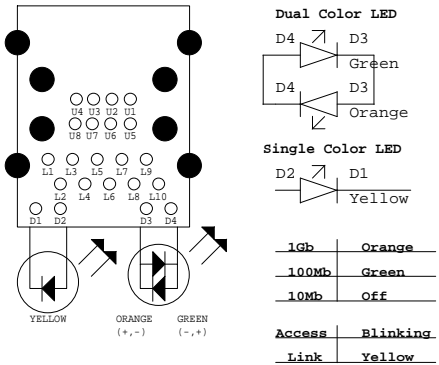
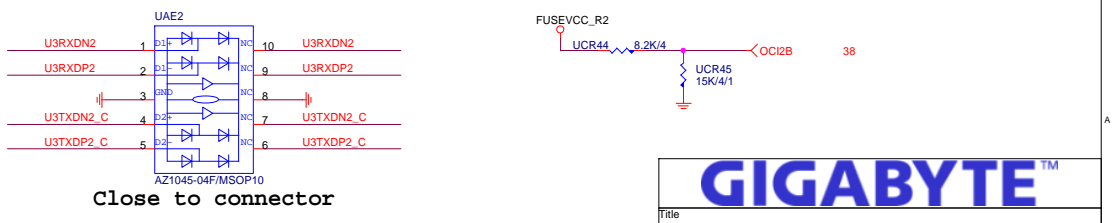
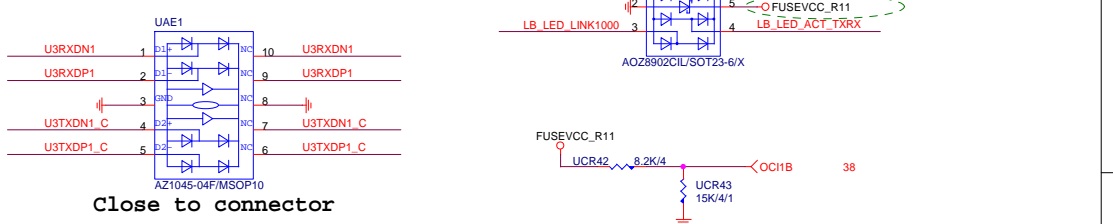
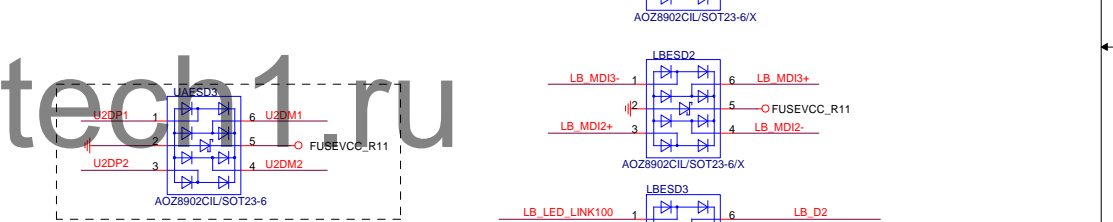
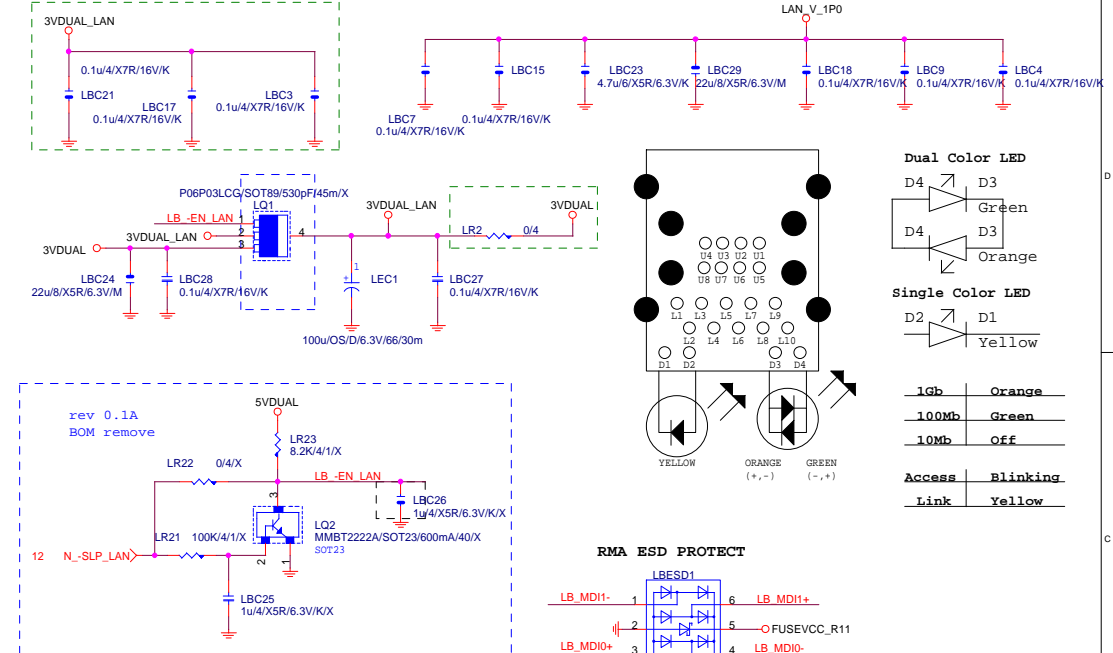
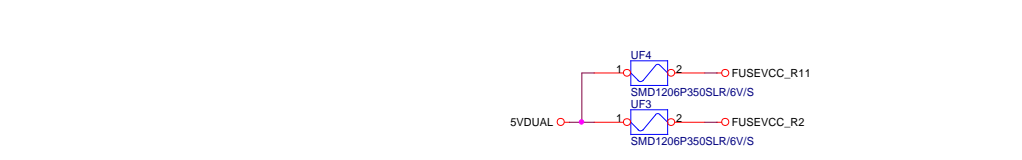
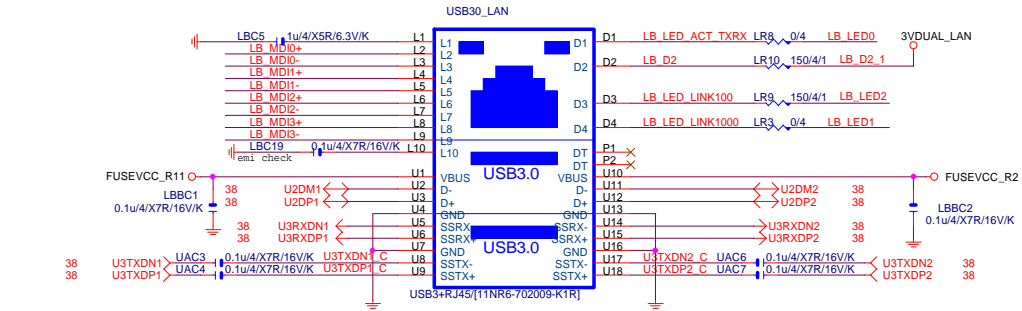
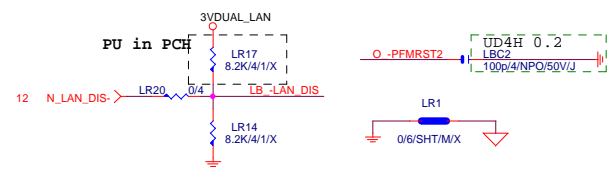
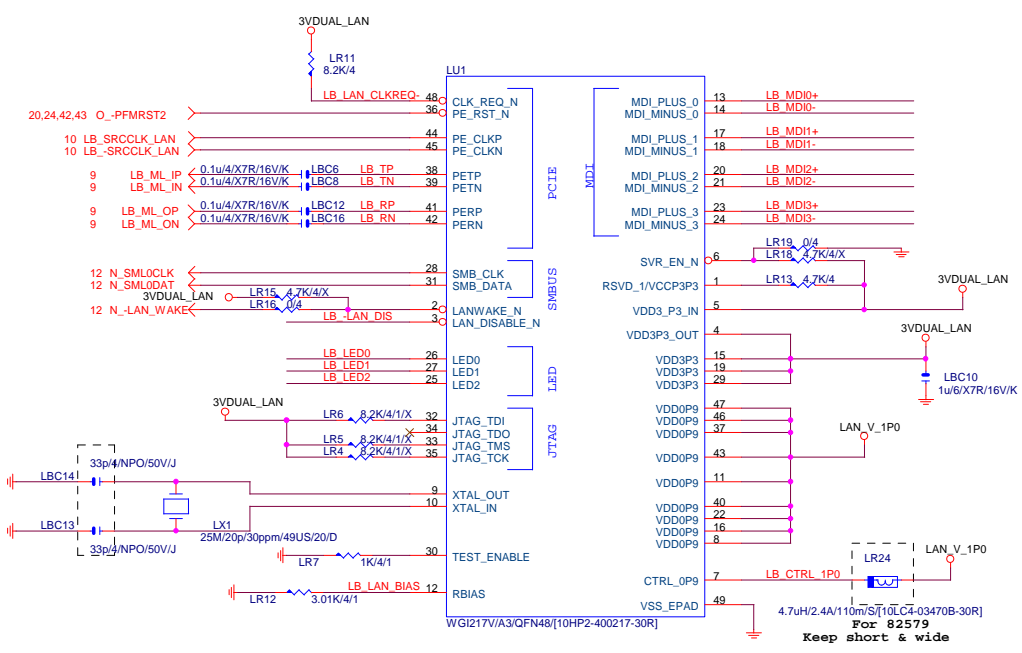


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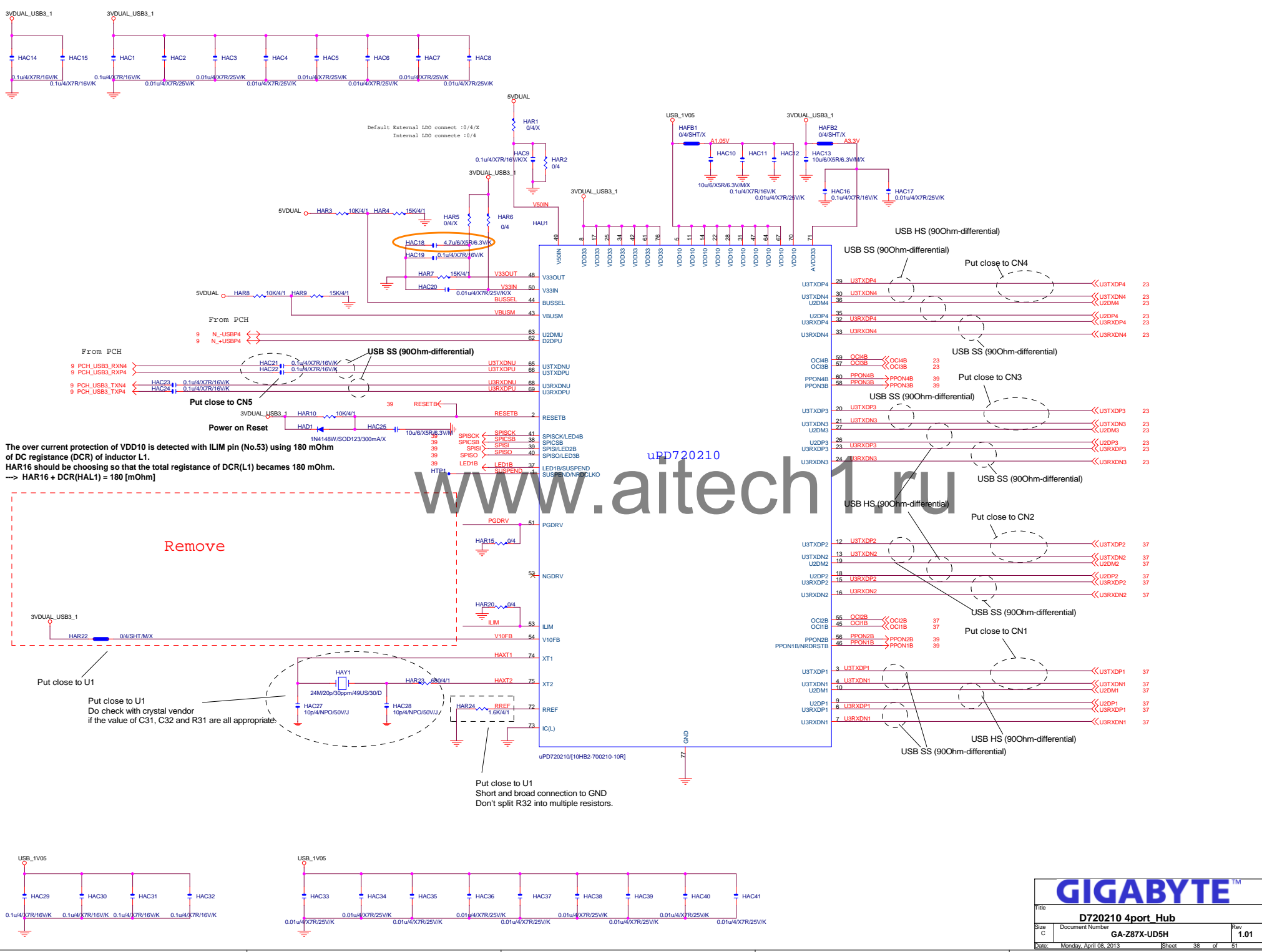
Title			DISCRETE POWER 2	
Size	Custom	Document Number	Rev	
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1.01

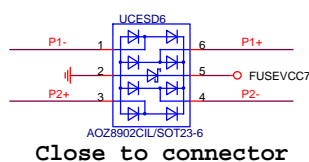
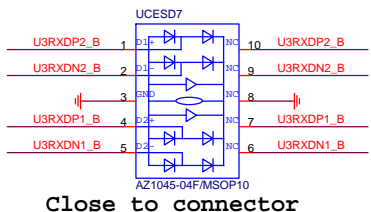
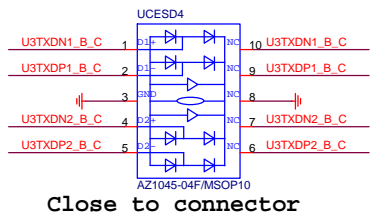
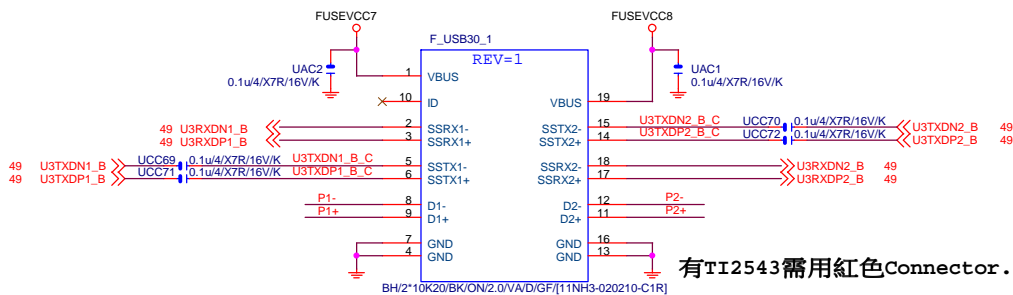


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Title		
INTEL LAN i217V		
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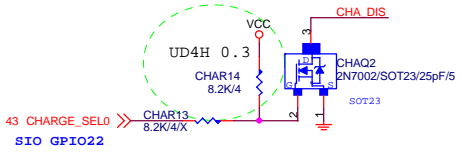
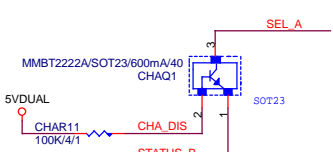
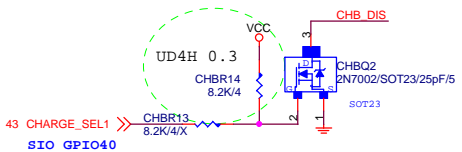
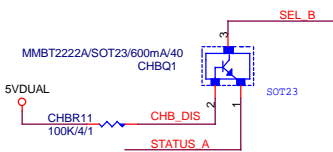
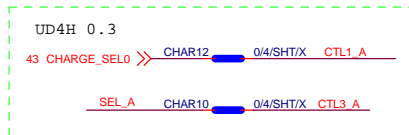
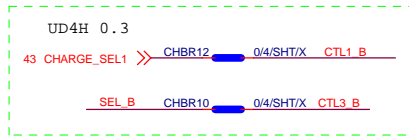
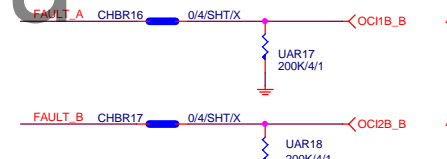
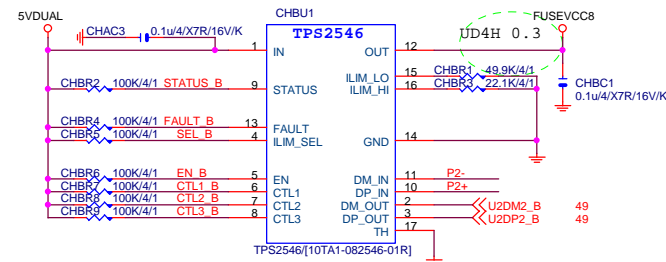
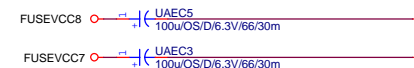
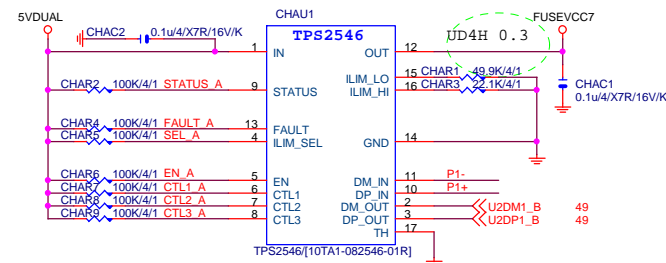


The schematic diagram illustrates the 3V3DUAL_USB circuit. It features a 5VDUAL input connected to a network of capacitors and a voltage regulator. The components and their values are as follows:

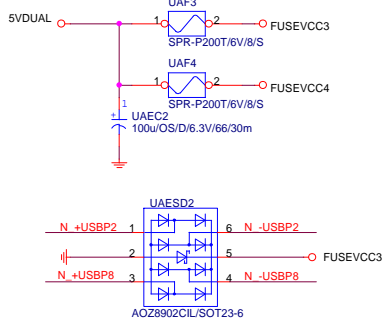
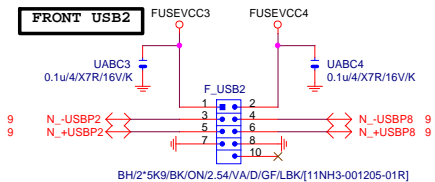
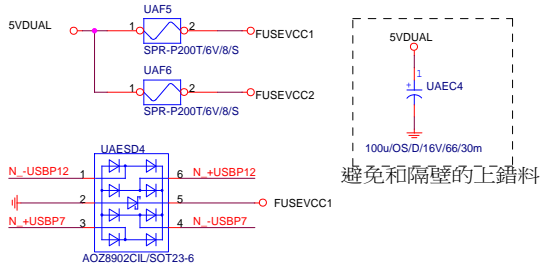
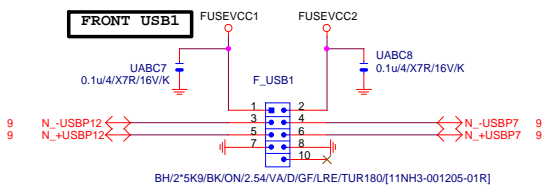
- 5VDUAL Input:** Connected to a network including capacitor HAC56 (0.1u/4/X7R/16V/K).
- HAQ3 L1085DG/TO252/5A:** A voltage regulator with its input connected to the 5VDUAL network and its output connected to the 3V3DUAL_USB3_1 output.
- Capacitors:**
 - HAC57 (1u/6/X7R/16V/K) is connected to the 5VDUAL input.
 - HAC58 (0.1u/4/X7R/16V/K) is connected to the 3V3DUAL_USB3_1 output.
 - HAC59 (0.1u/4/X7R/16V/K) is connected to the output of the HAQ3 regulator.
 - HAEC2 (100uFP/D/6.3V/65°C/13m) is connected to the 3V3DUAL_USB3_1 output.
- Resistors:**
 - HAR51 (100/4/1) is connected to the output of the HAQ3 regulator.
 - HAR52 (169/4/1) is connected to the output of the HAQ3 regulator.



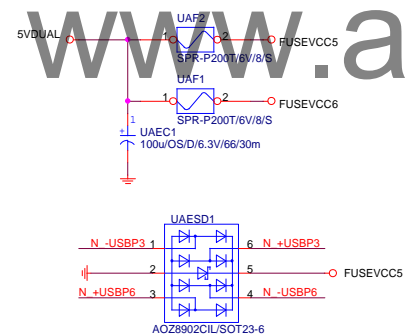
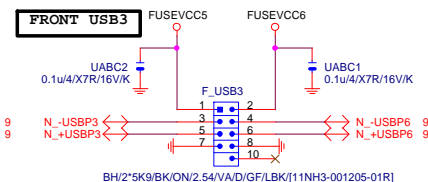
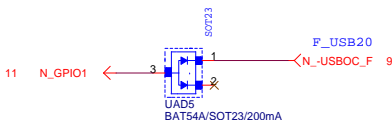
TI2543內建Fuse，移除UAFB1~2.



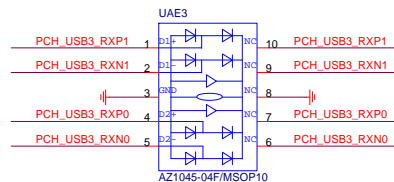
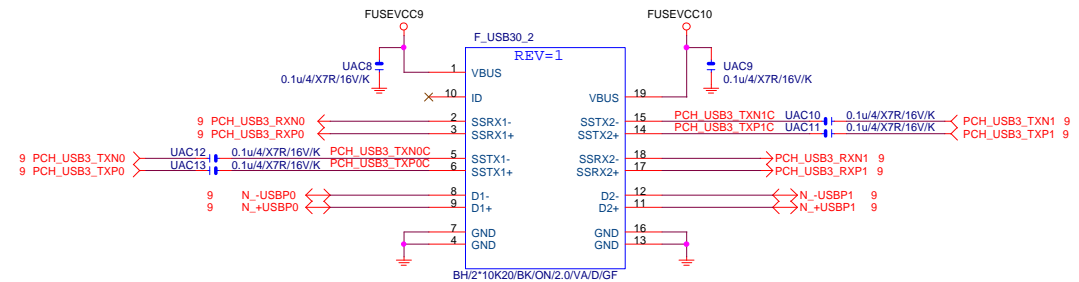
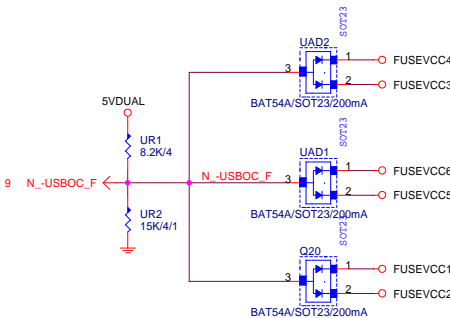
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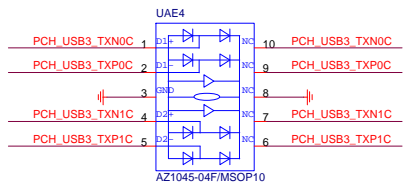
Close to connector



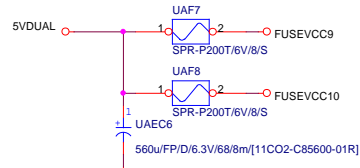
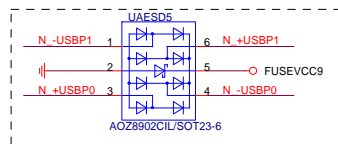
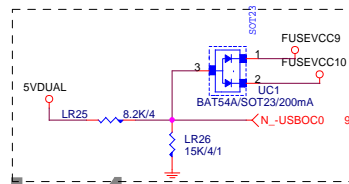
Close to connector



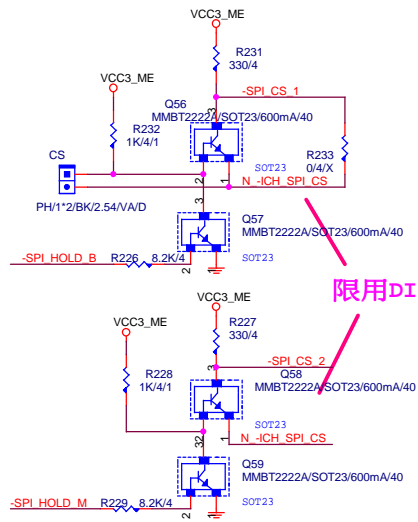
Close to connector



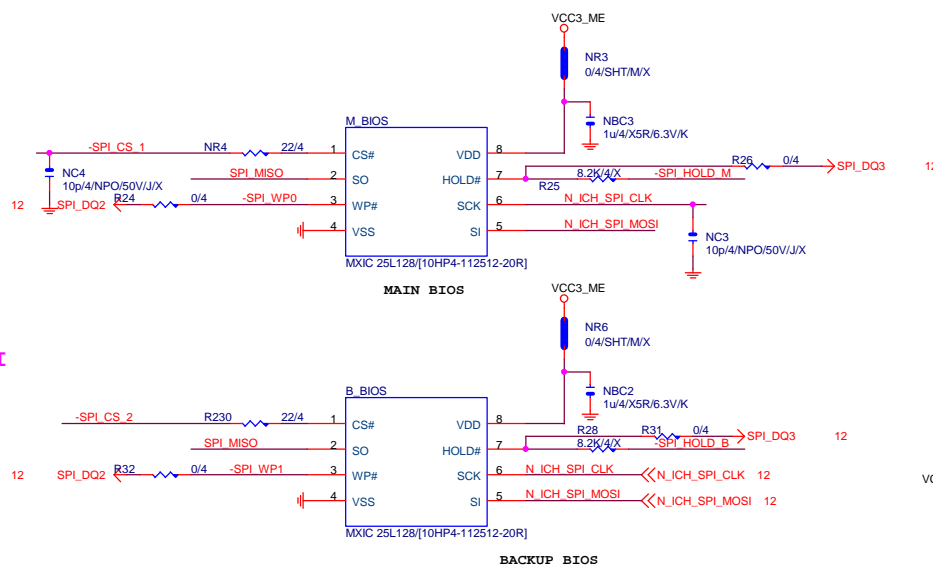
Close to connector



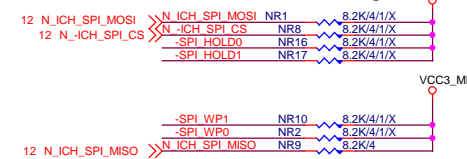
GIGABYTE™		
Title	FRONT USB 2.0, F_USB30_2	
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限用DII



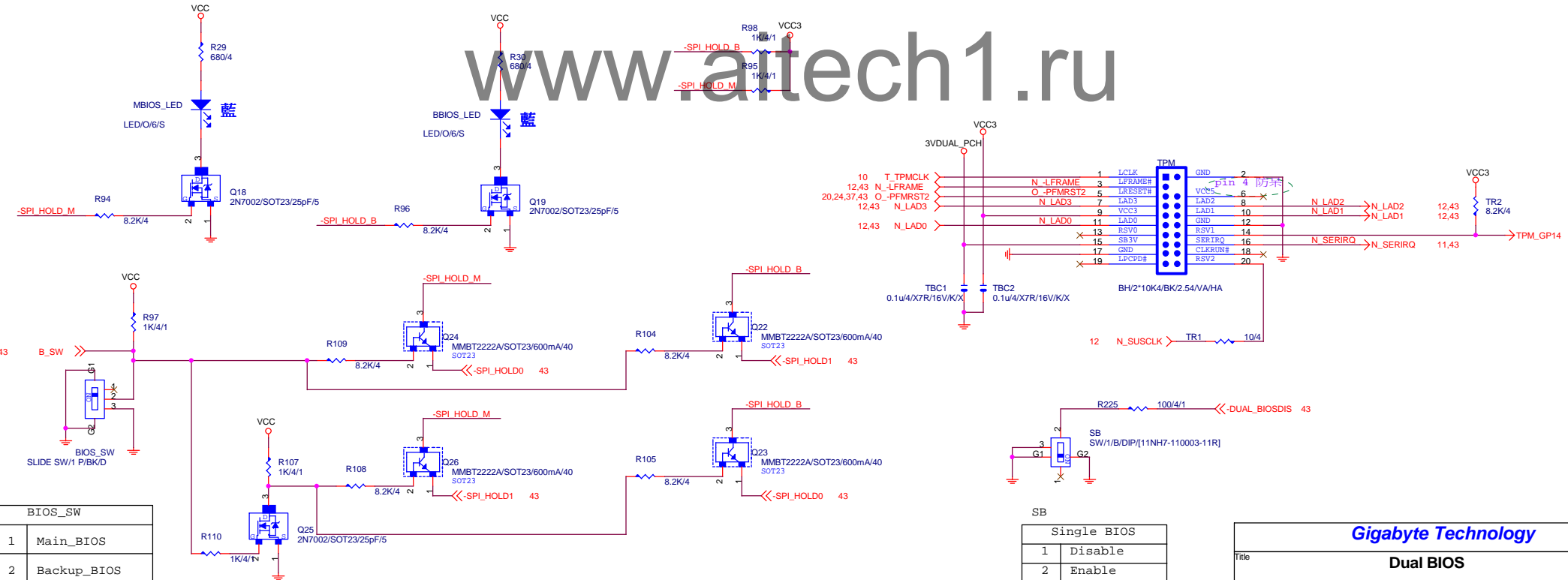
MOSI For DMI RX Termination Voltage



1 means floating
0 means PD 1K

BOOT	GNT0	GNT1
DEVICE		
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

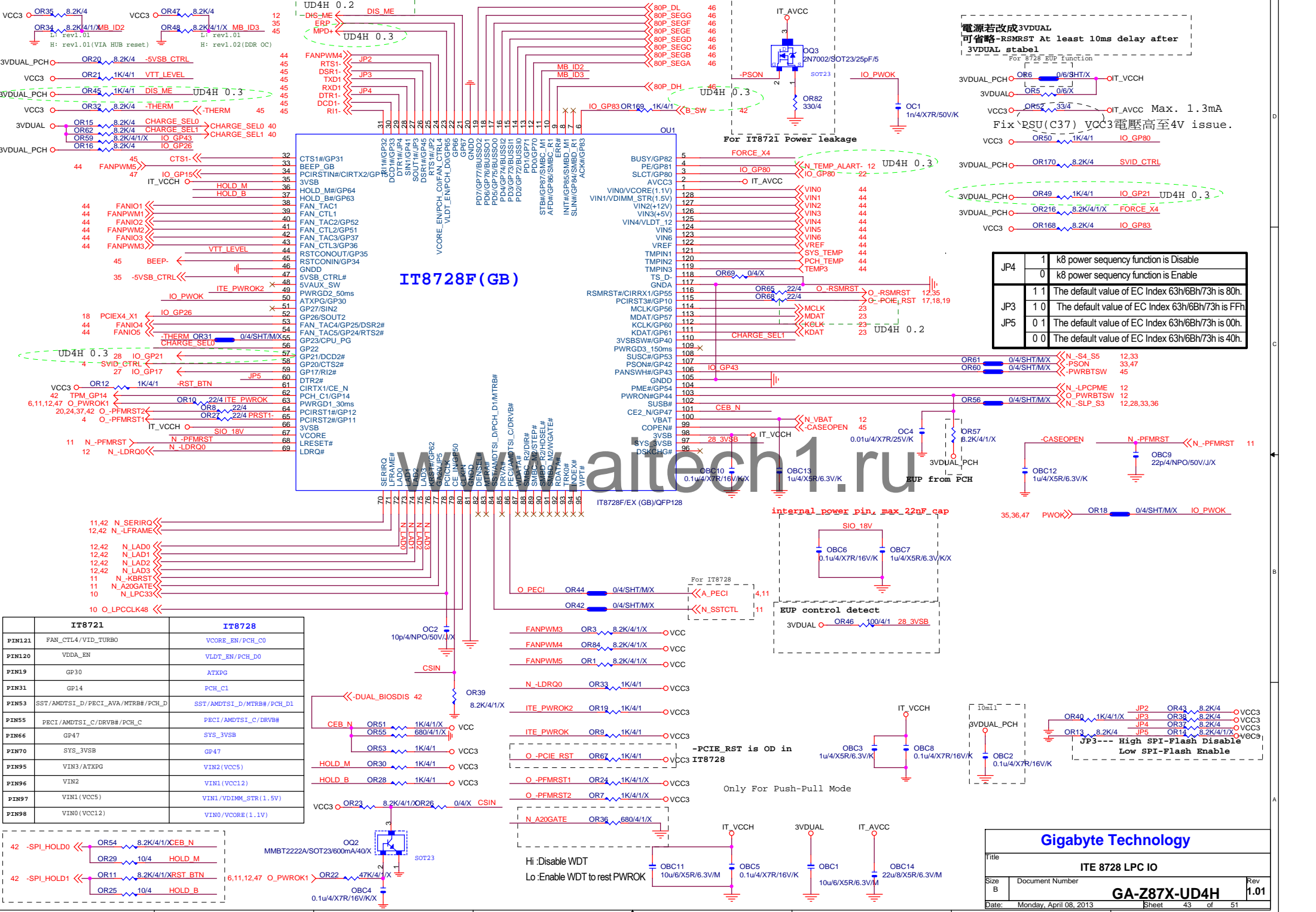
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BIOS_SW	
1	Main_BIOS
2	Backup_BIOS

SB	
1	Disable
2	Enable

Gigabyte Technology		
Title		
Dual BIOS		
Size	Document Number	Rev
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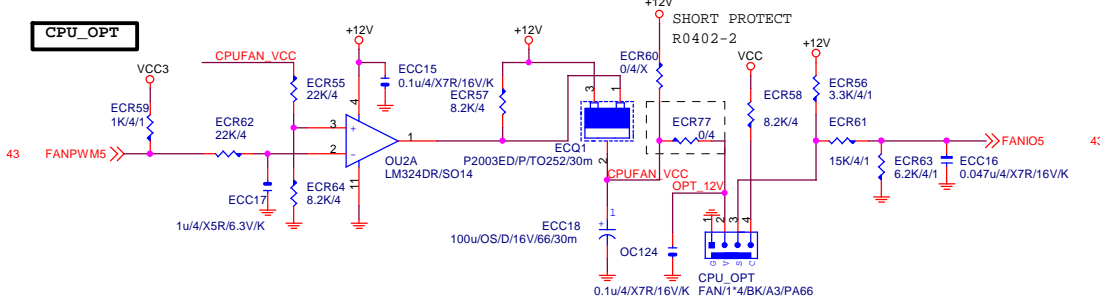


電源若改成3VDUAL
可省略-RSMRST At least 10ms delay after
3VDUAL stabel
For 8728 EUP Function
3VDUAL_PCH OR20 8.2K/4 -5VSB_CTRL
3VDUAL OR5 0.6/X
VCC3 OR5 33/4
VCC3 OR50 1K/4/1 IO GP80
Fix PSU(C37) VCC3電壓高至4V issue.

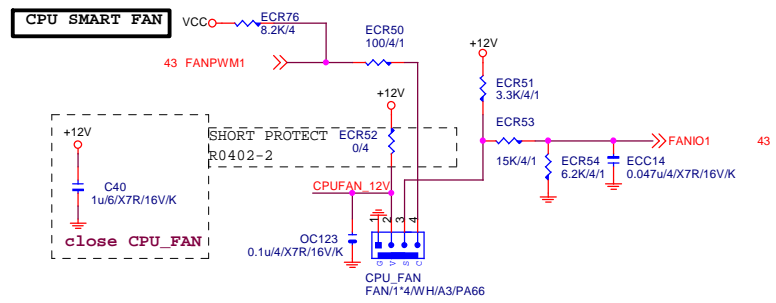
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

	IT8721	IT8728
PIN121	FAN_CTL4/VID_TURBO	VCORE_EN/PCH_C0
PIN120	VDDA_EN	VLDI_EN/PCH_D0
PIN19	GP30	ATXP_G
PIN31	GP14	PCH_C1
PIN53	SST/AMDTSI_D/PECI_AVA/MTRB#/PCH_D	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSI_C/DRV#/PCH_C	PECI/AMDTSI_C/DRV#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3/ATXP_G	VIN2(VCC5)
PIN96	VIN2	VIN1(VCC12)
PIN97	VIN1(VCC5)	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0(VCC12)	VIN0/VCORE(1.1V)

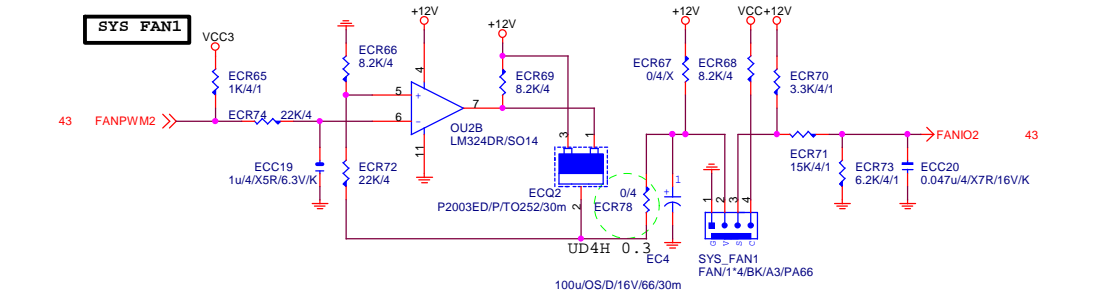
CPU_OPT



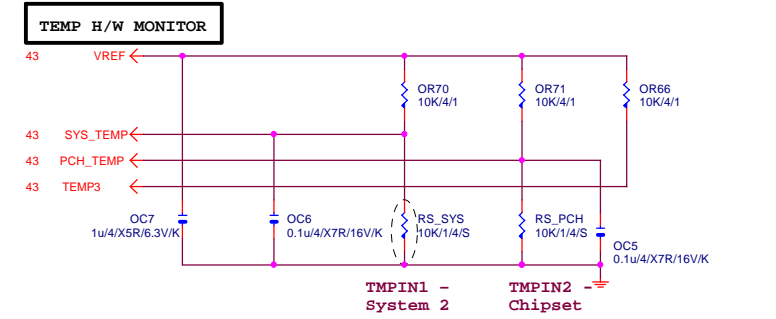
CPU SMART FAN



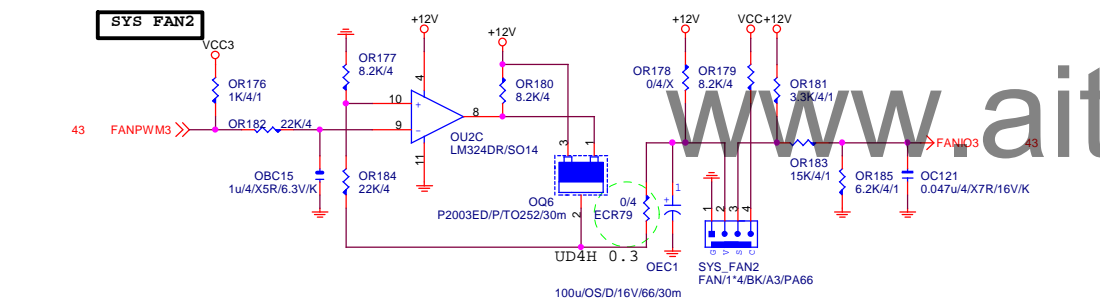
SYS_FAN1



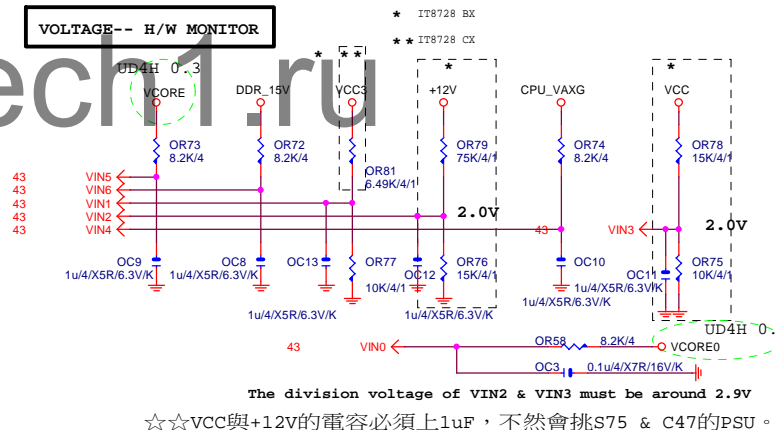
TEMP H/W MONITOR



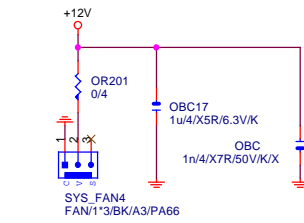
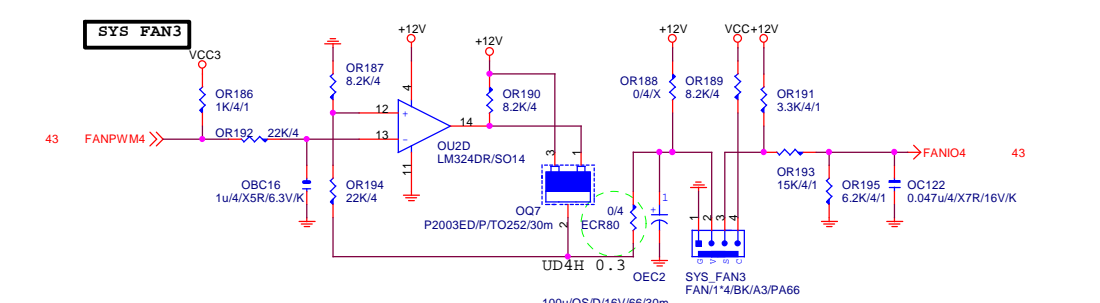
SYS_FAN2



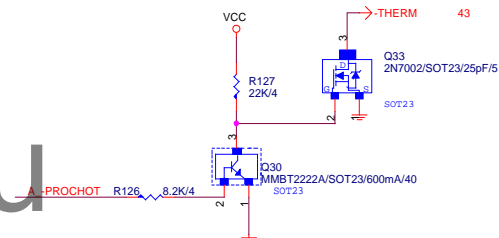
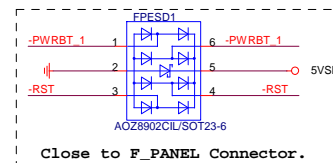
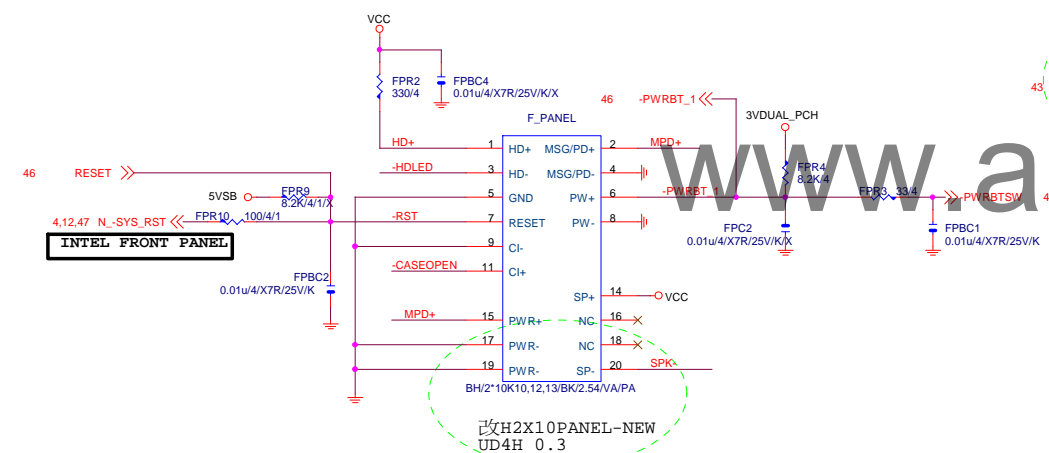
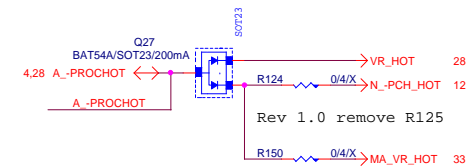
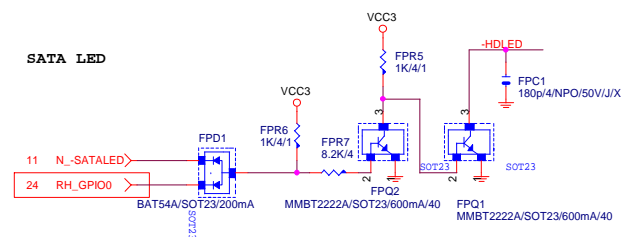
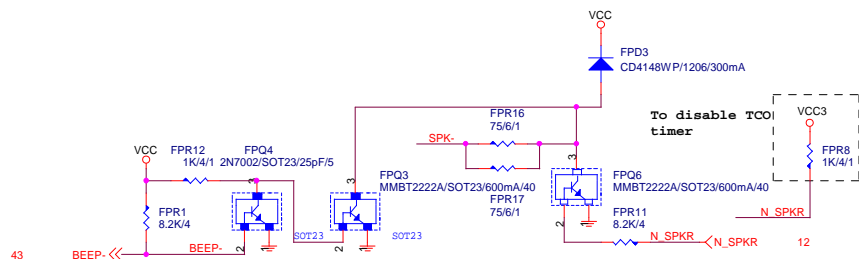
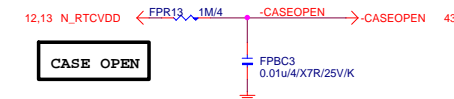
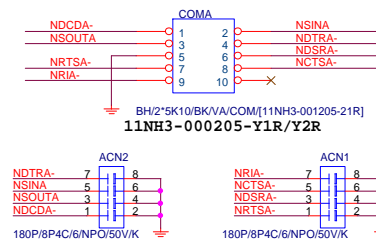
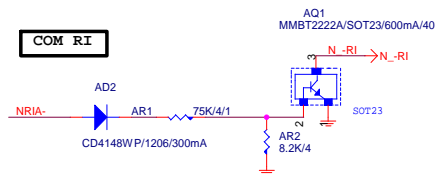
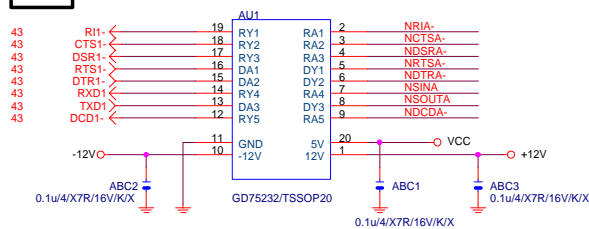
VOLTAGE-- H/W MONITOR



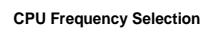
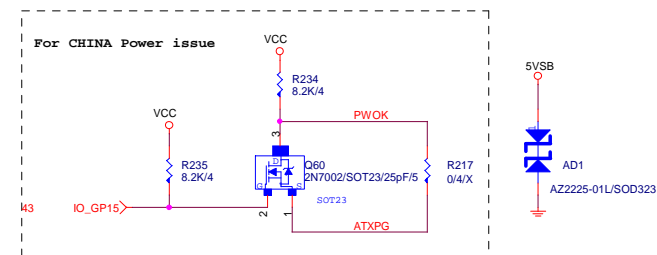
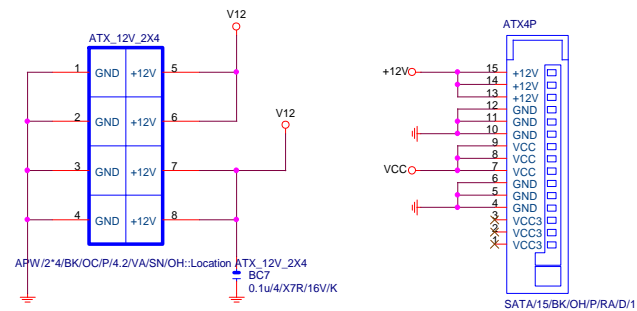
SYS_FAN3



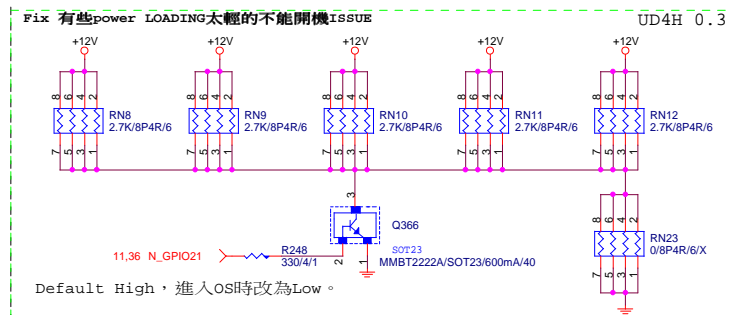
Gigabyte Technology			
Title HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
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Title R&D 155



CLK GEN CK505



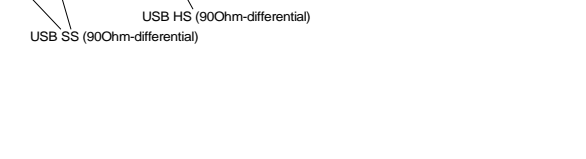
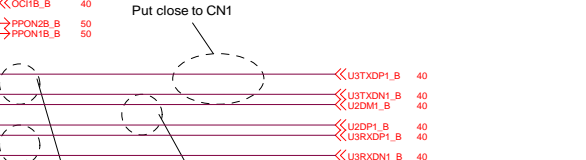
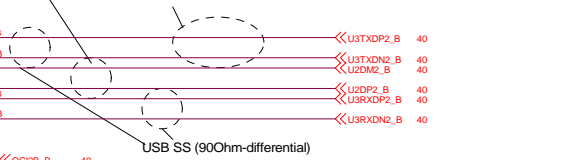
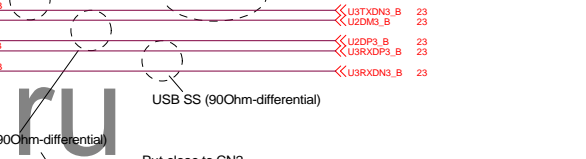
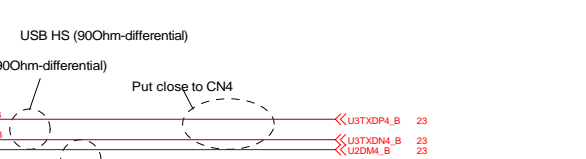
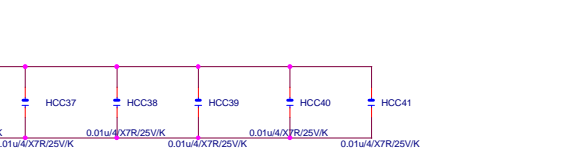
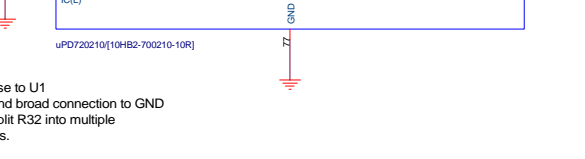
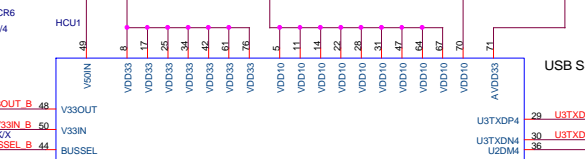
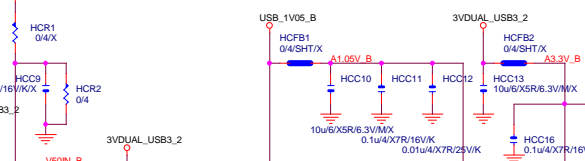
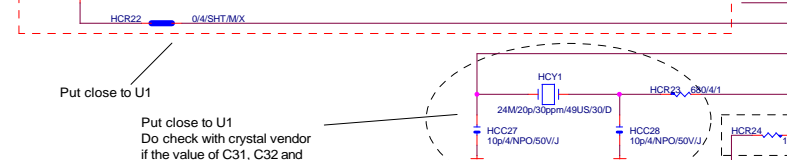
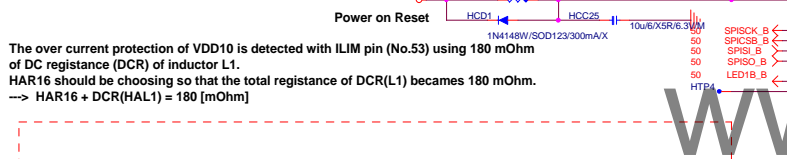
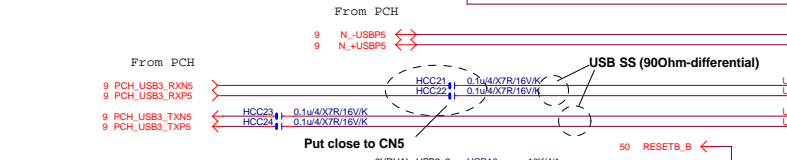
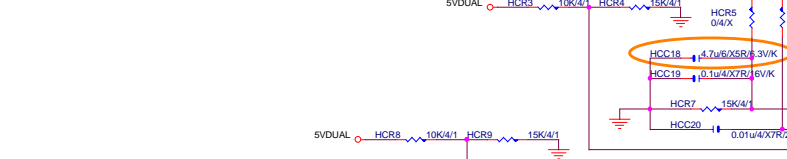
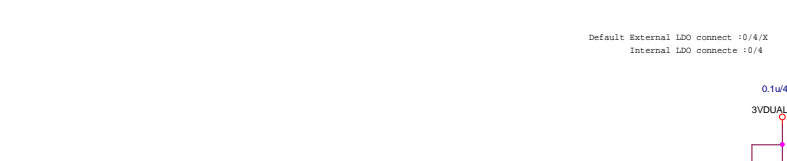
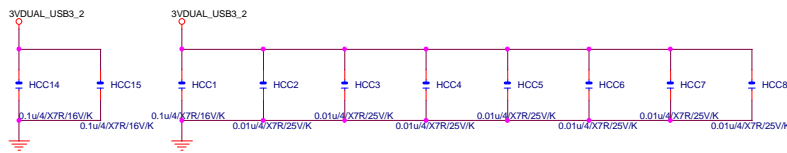
Gigabyte Technology

Title			
ATX POWER CONNECTOR			
Size Custom	Document Number	GA-Z87X-UD4H	Rev 1.01
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散熱模組料號:

2R
2R



The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]

Remove

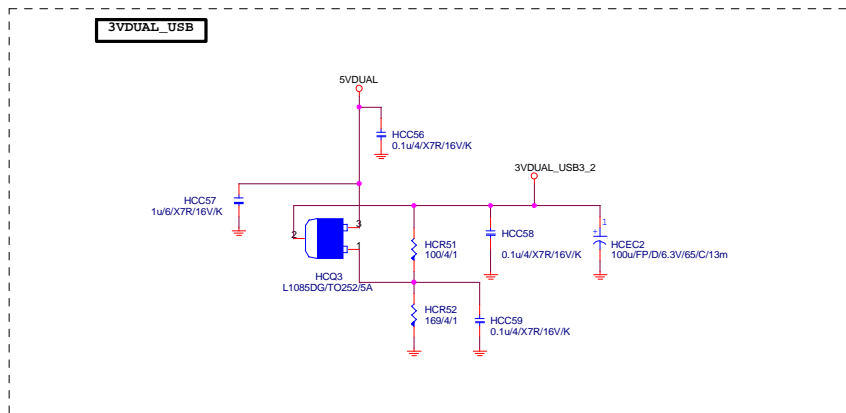
Put close to U1
Do check with crystal vendor
if the value of C31, C32 and
R31 are all appropriate.

Put close to U1
Short and broad connection to GND
Don't split R32 into multiple
resistors.

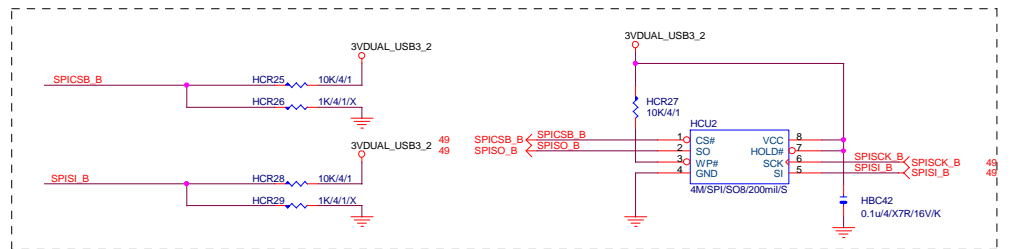
uP720210

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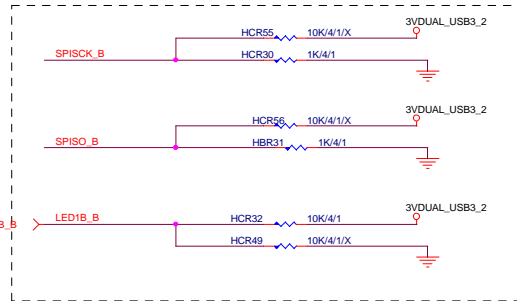
GIGABYTE™			
Title			
D720210 4port Hub B			
Size	Document Number	Rev	
C	GA-Z87X-UD4H	1.01	
Date:	Monday, April 08, 2013	Sheet	49 of 51



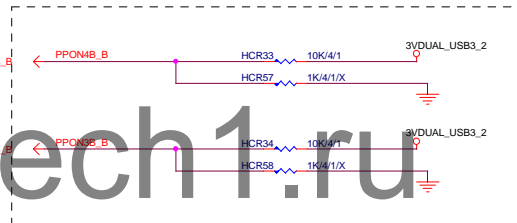
External SPI ROM ; SPI ROM attached mode



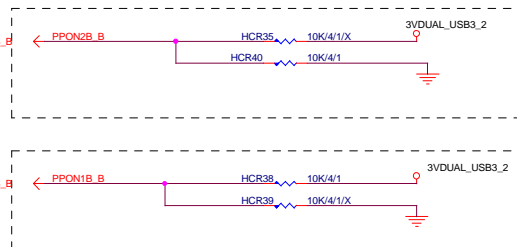
Battery Charging



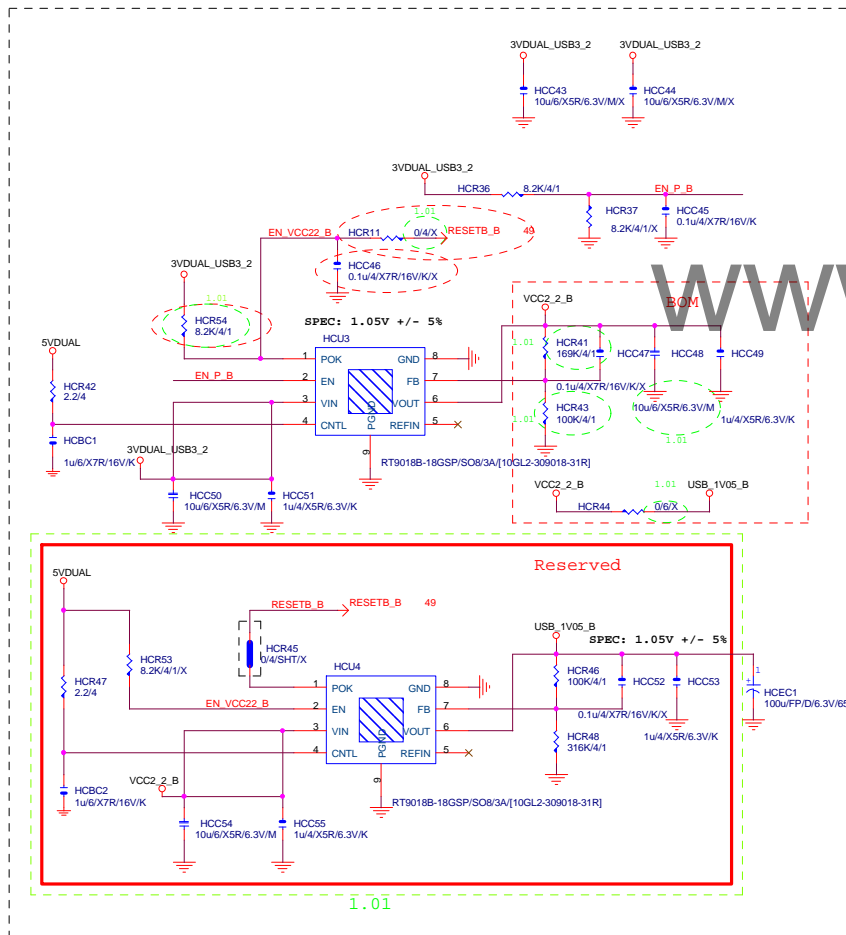
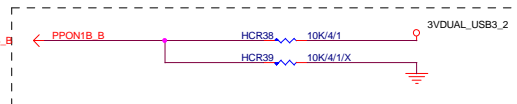
Number of Ports ; 4Ports mode

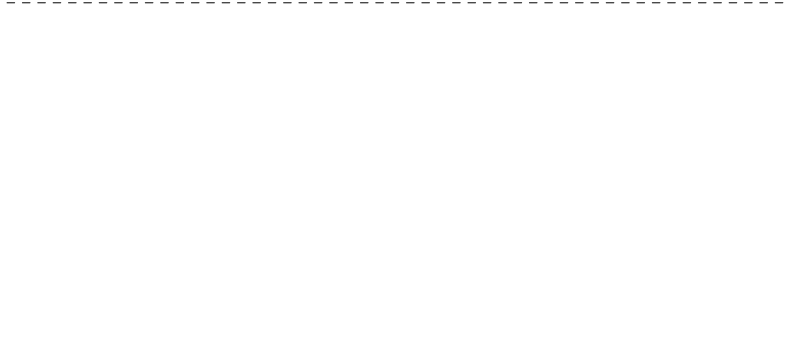
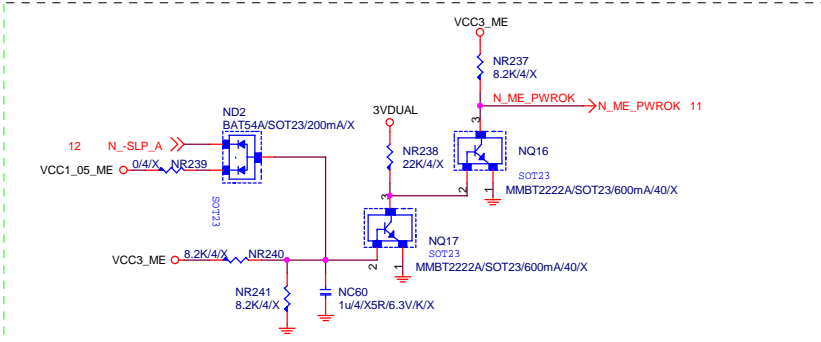
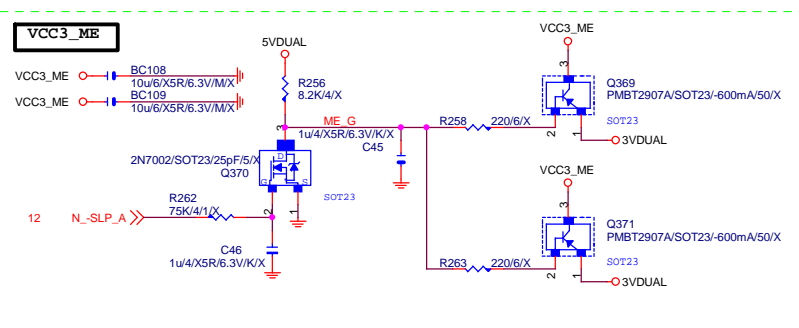
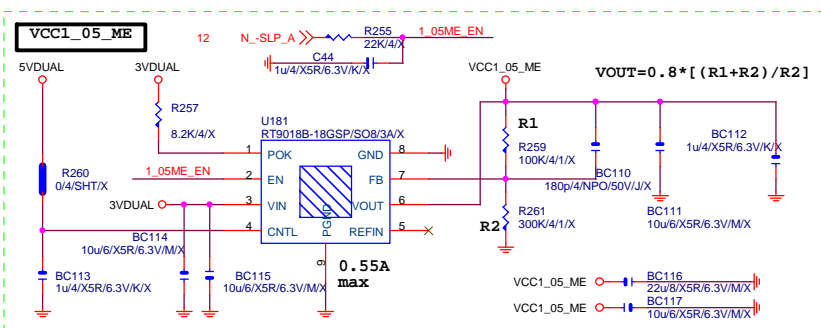


#5 VBUS Power Control ; Individual mode



PPON1B Pin Function ; Port1 PPONB mode





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